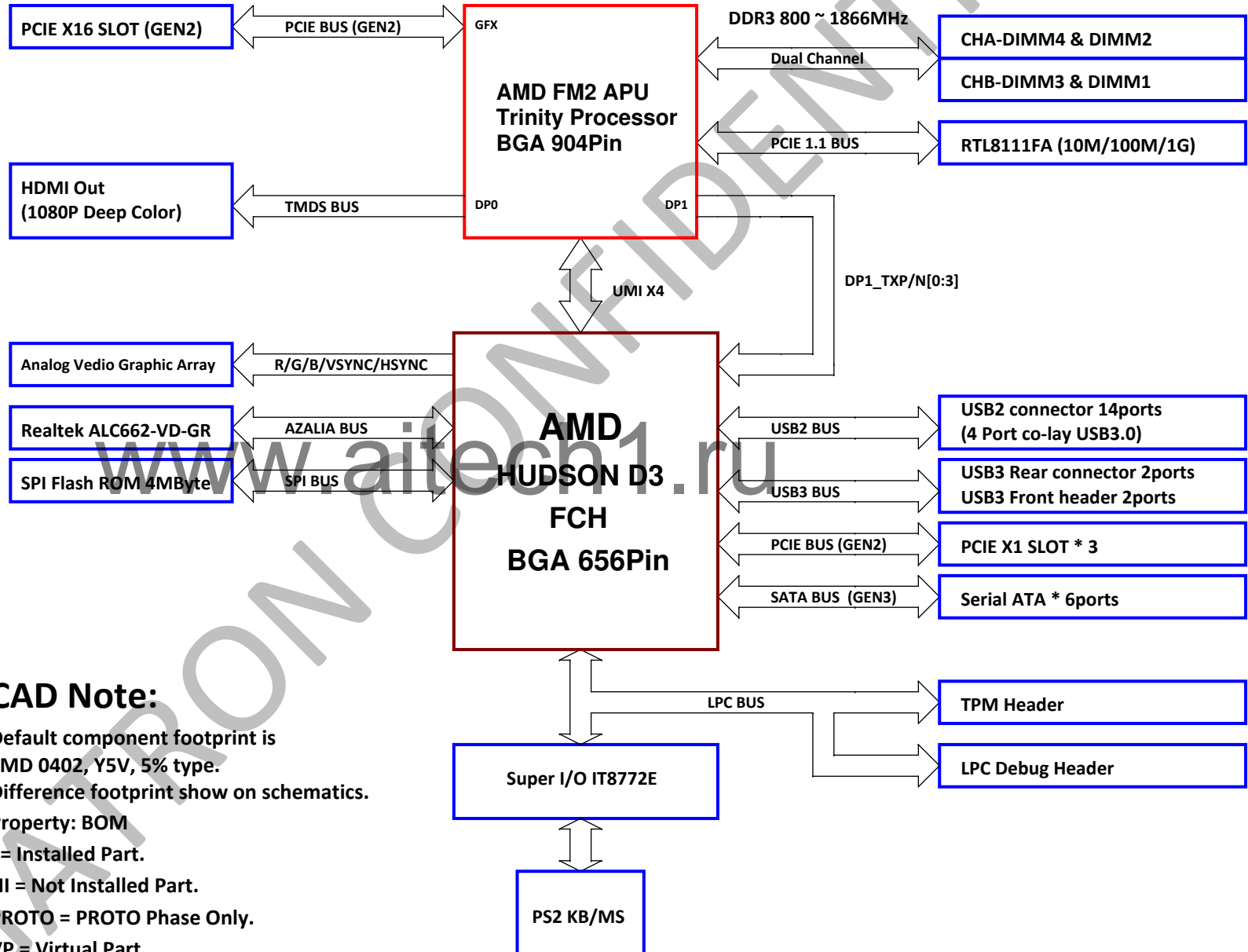


PAGE	TITLE
01	Block Diagram
02	ECN CONTR TABLE&CHANGE HISTORY
03	POWER DISTRIBUTION
04	CLOCKS DISTRIBUTION
05	POWER & SIGNAL & RESET MAP
06	POWER_FLOWCHART
07	POWER SEQUENCE
08	AMD_FM2_SOCKET_GFX&GPP&UMI
09	AMD_FM2_SOCKET_DDR3
10	AMD_FM2_SOCKET_DP&MISC
11	AMD_FM2_SOCKET_POWER
12	DDR3_CHANNEL_A
13	DDR3_CHANNEL_B
14	DDR3 DECOUPLING CAP
15	FCH_Hudson-D3_UMI&GPP&CLK&PCI
16	FCH_HudsonD3_MISC&AUDIO&USB
17	FCH_HudsonD3_SATA&SD&LAN&VGA
18	FCH_HudsonD3_POWER
19	FCH_HudsonD3_HWSTRAP
20	INTEGRATED GRAPHICS VGA
21	HDMI OUT CONNECTOR
22	PCI EXPRESS X16 SLOT
23	PCI EXPRESS X1 SLOT1
24	PCI EXPRESS X1 SLOT2
25	PCI EXPRESS X1 SLOT3
26	REALTEK RTL8111E
27	REAR RJ-45+USB 3.0 CONNECTOR
28	REAR QUAL USB 2.0 CONNECTOR
29	FRONT USB 2.0 HEADER * 3
30	FRONT USB 3.0 HEADER
31	USB 3.0 PORT CHARGER
32	SATA CONNECTOR * 6
33	REALTEK ALC662 AZALIA CODEC
34	FRONT AUDIO CONNECTOR
35	REAR AUDIO CONNECTOR
36	INT-SPK & SPDIF OUT HEADER
37	COM PORT (RESERVE)
38	SUPER I/O - IT8772E
39	FRONT PANEL
40	BOARD ID + BUZZER + SCREW
41	SPI ROM & RTC
42	KB/MS & TPM & EUP CONTROL
43	SYS & CPU_FAN
44	ATX POWER
45	VCORE CONTROLLER
46	VCORE DRIVER1
47	VCORE DRIVER2
48	VDDNB
49	VDDP&VDDR
50	+1P5V_DUAL&+VTT_DDR
51	+5V_DUAL &+ 3P3VSB/+1P1VSB
52	PROCHOT#&+1P1V&+2P5V



CAD Note:

Default component footprint is
SMD 0402, Y5V, 5% type.
Difference footprint show on schematics.

Property: BOM

I = Installed Part.

NI = Not Installed Part.

PROTO = PROTO Phase Only.

VP = Virtual Part.

PAGE	TITLE
53	53.EMI & STITCHING CAP

16GB Max Memory Support

MEMORY UNBUFFER-DIMM*4

CHA-DIMM4 & DIMM2

CHB-DIMM3 & DIMM1

RTL8111FA (10M/100M/1G)

USB2 connector 14ports
(4 Port co-lay USB3.0)

USB3 Rear connector 2ports
USB3 Front header 2ports

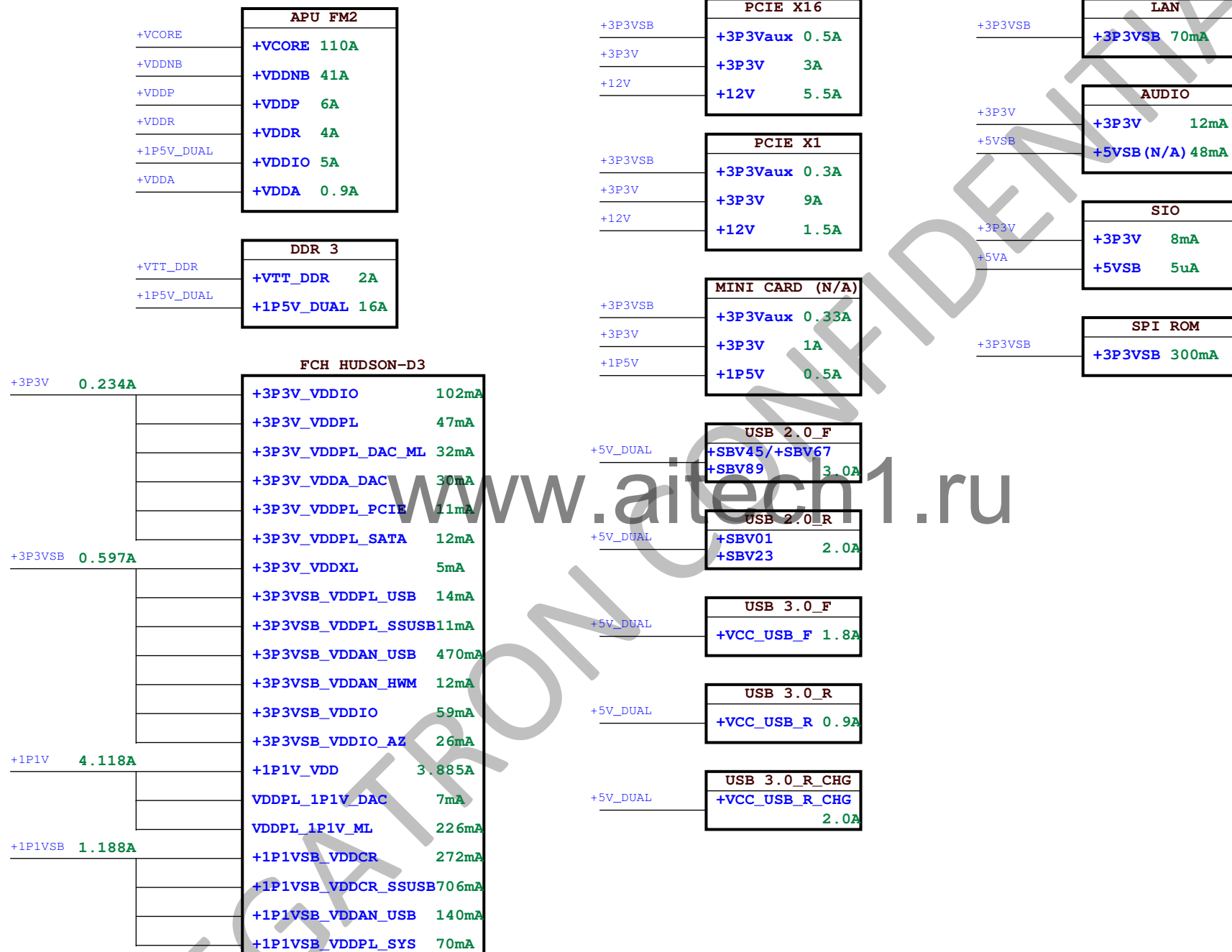
PCIE X1 SLOT * 3

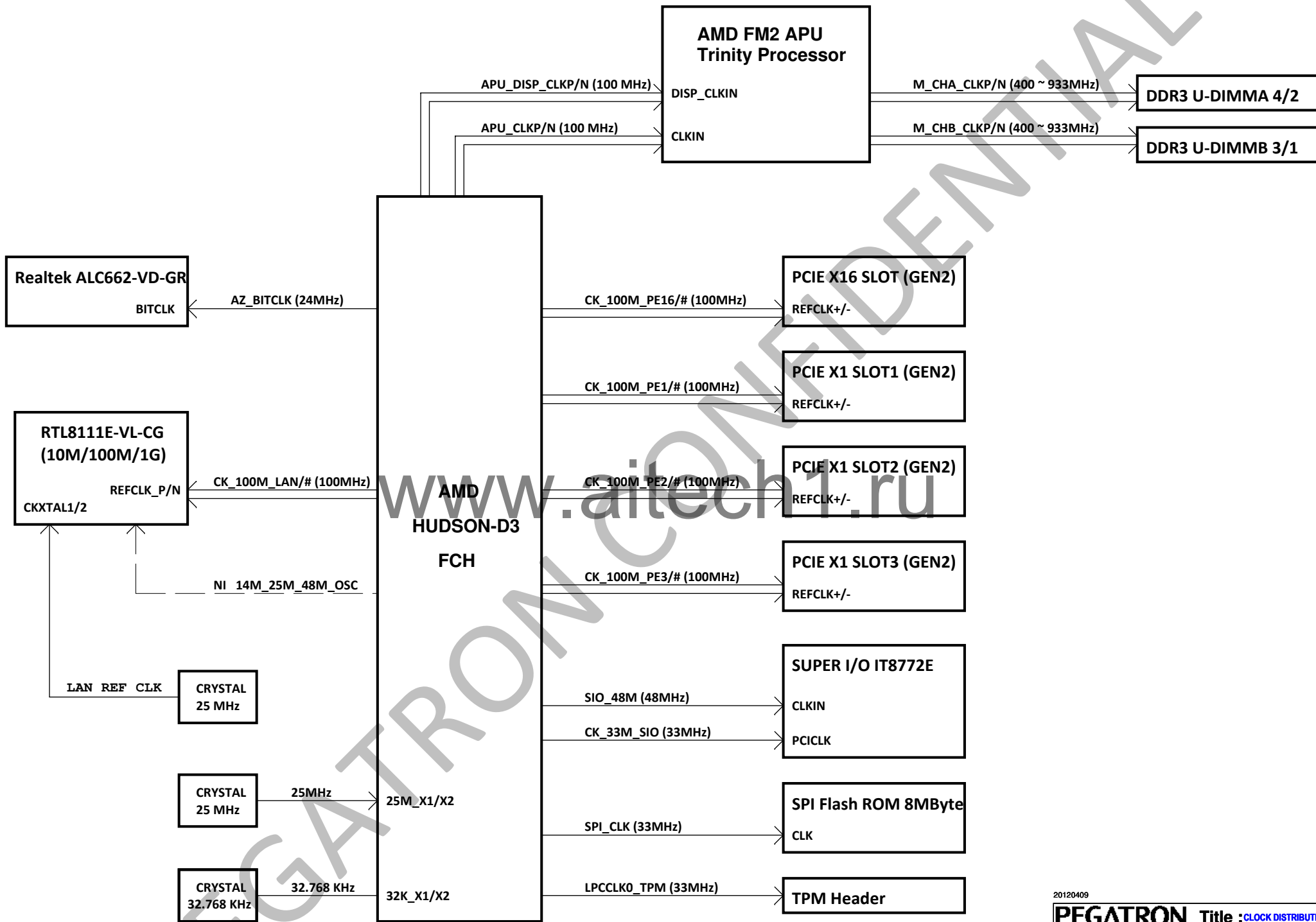
Serial ATA * 6ports

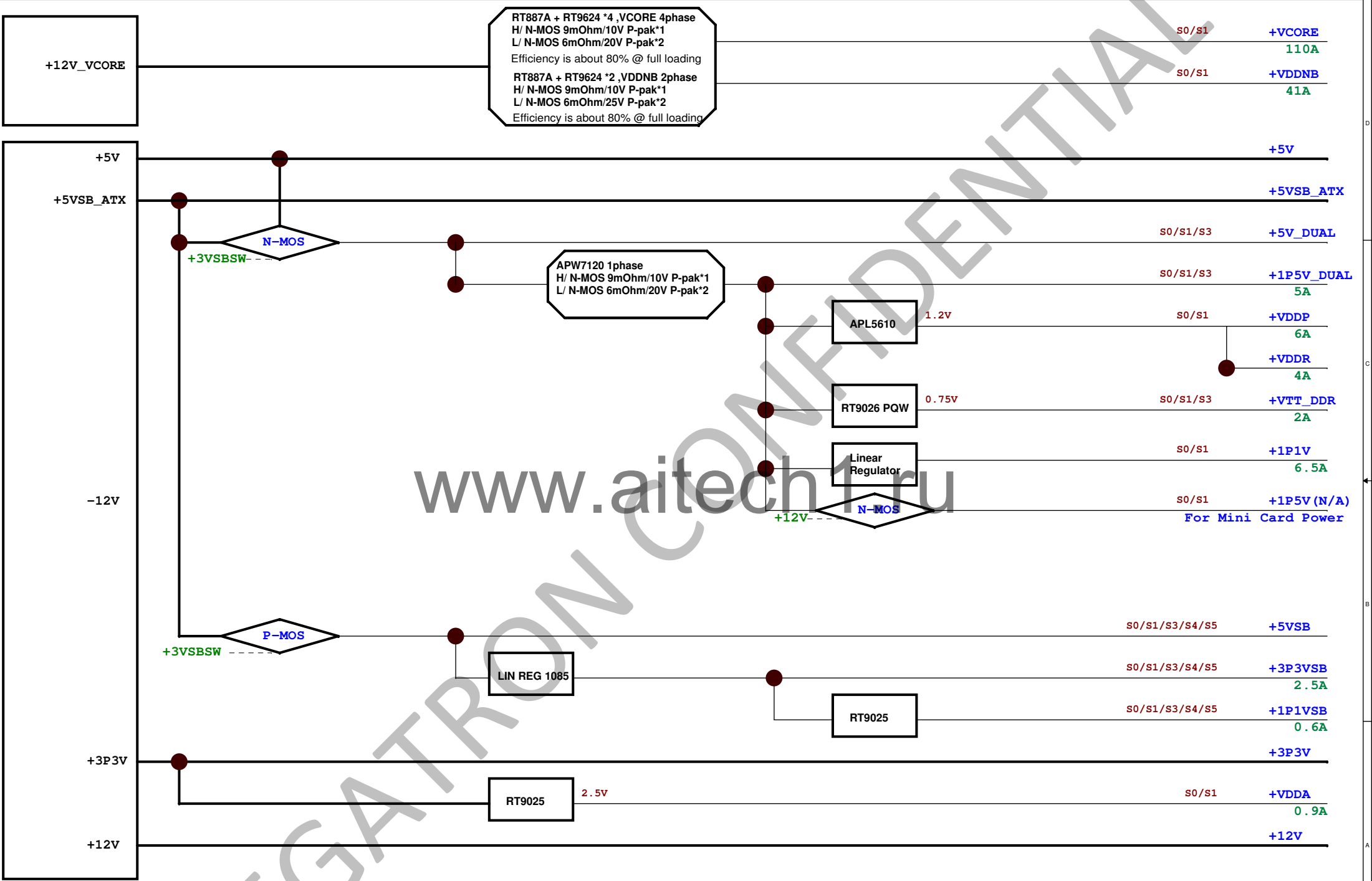
TPM Header

LPC Debug Header

Power Distribution







RT887A + RT9624 *4 ,VCORE 4phase
H/ N-MOS 9mOhm/10V P-pak*1
L/ N-MOS 6mOhm/20V P-pak*2
Efficiency is about 80% @ full loading

RT887A + RT9624 *2 ,VDDNB 2phase
H/ N-MOS 9mOhm/10V P-pak*1
L/ N-MOS 6mOhm/25V P-pak*2
Efficiency is about 80% @ full loading

APW7120 1phase
H/ N-MOS 9mOhm/10V P-pak*1
L/ N-MOS 6mOhm/20V P-pak*2

APL5610

RT9026 PQW

Linear
Regulator

LIN REG 1085

RT9025

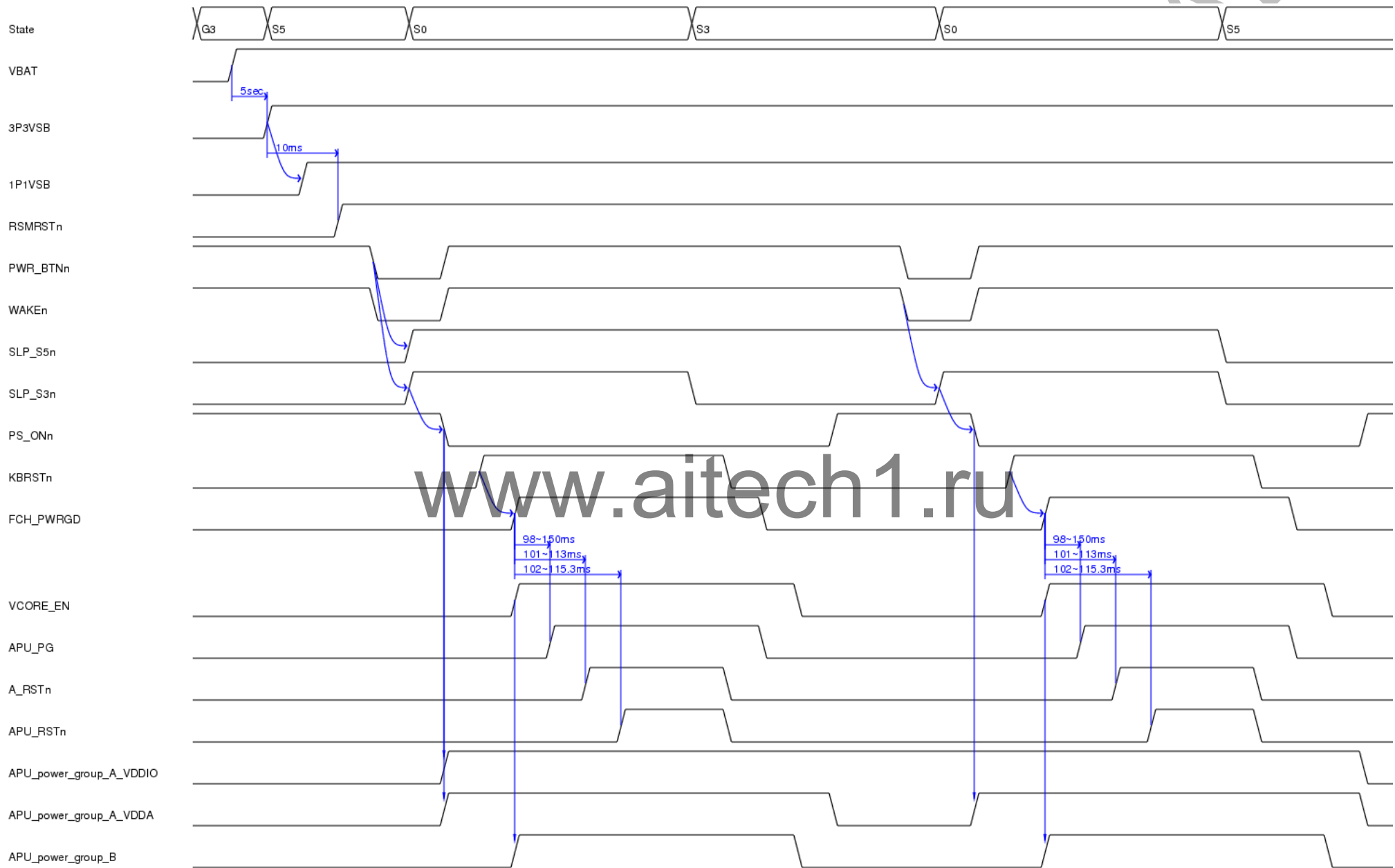
RT9025

Switch ON/OFF

Switching

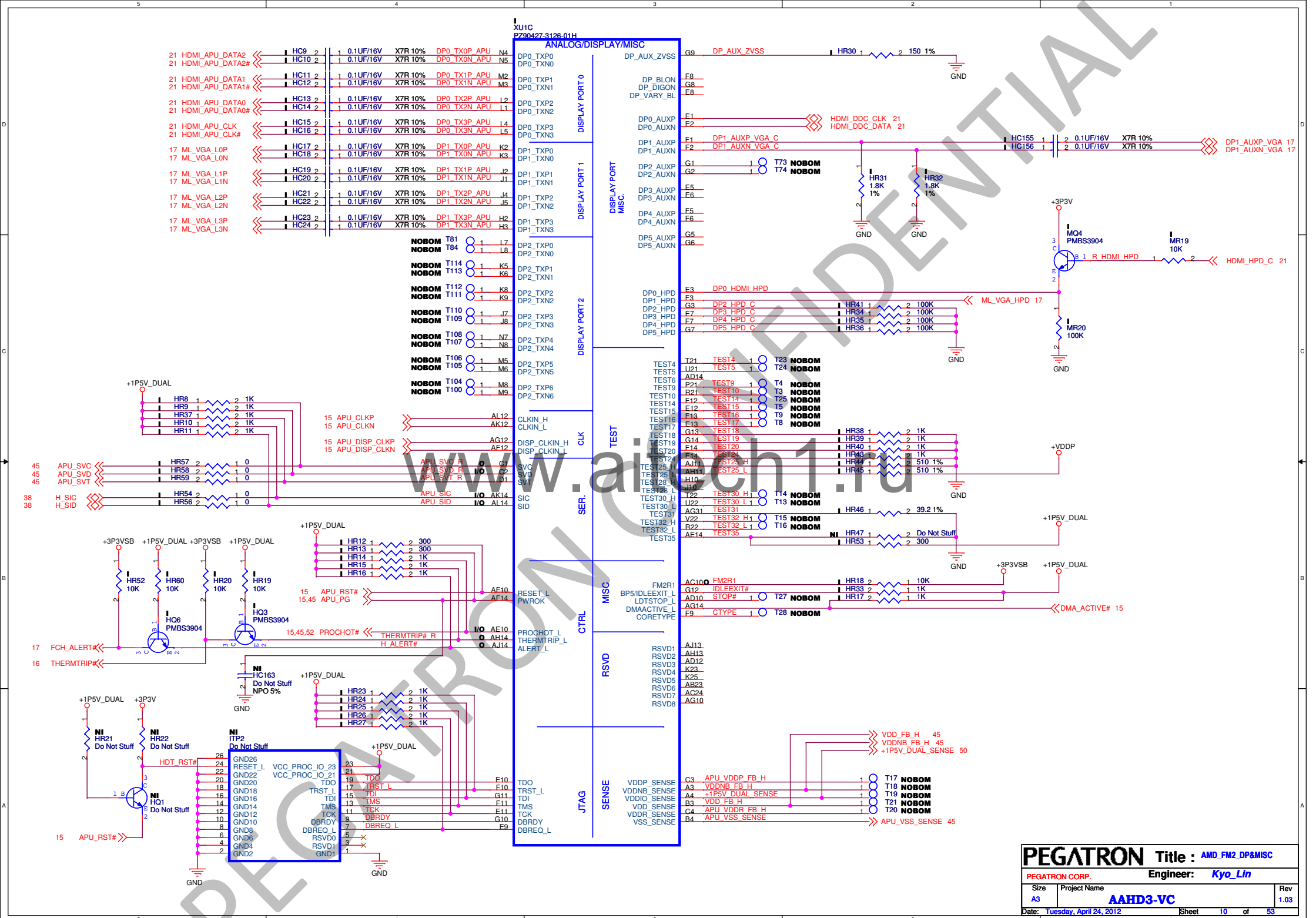
Linear

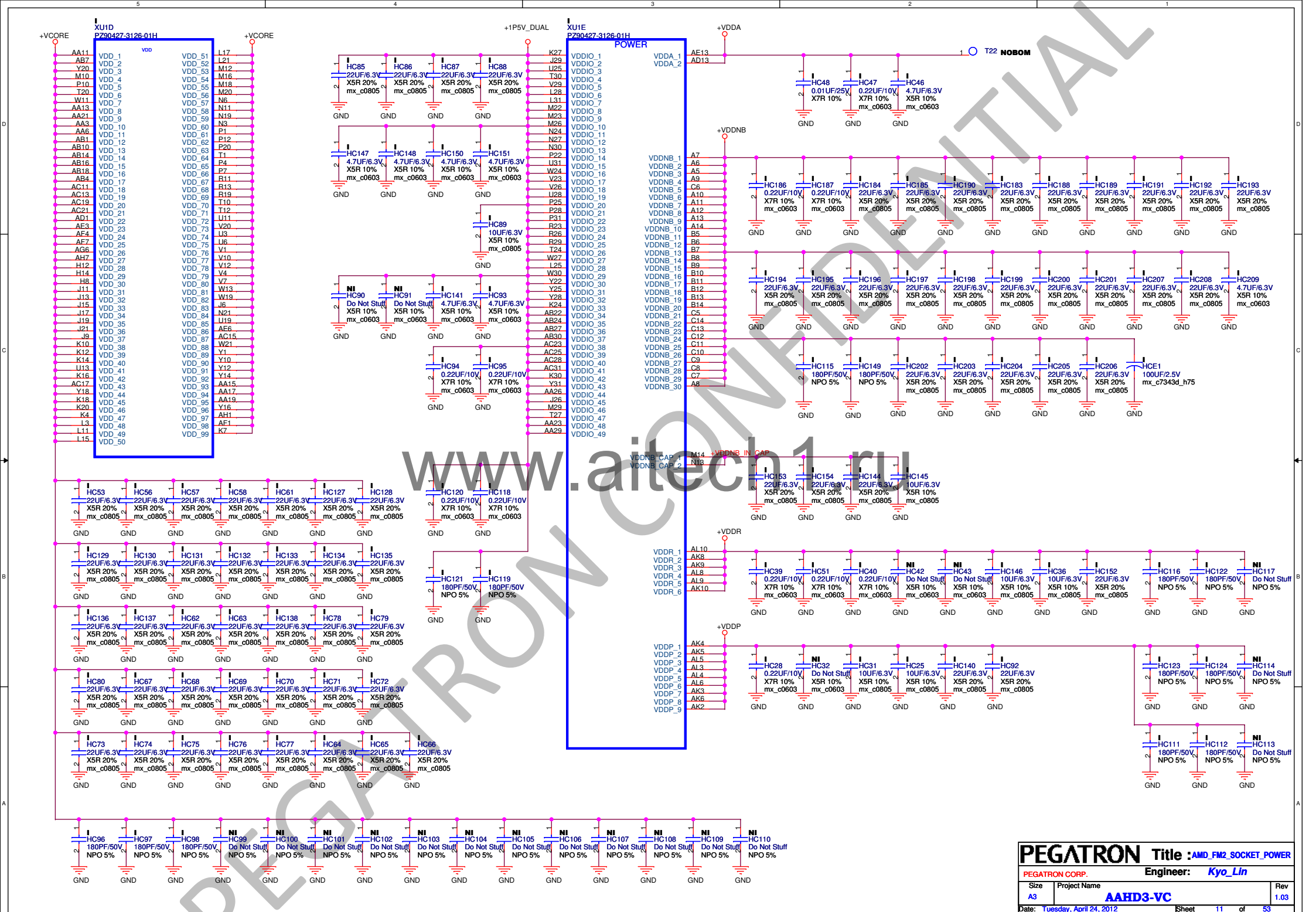
Note: lxx/loo
means
ltdc/lmax

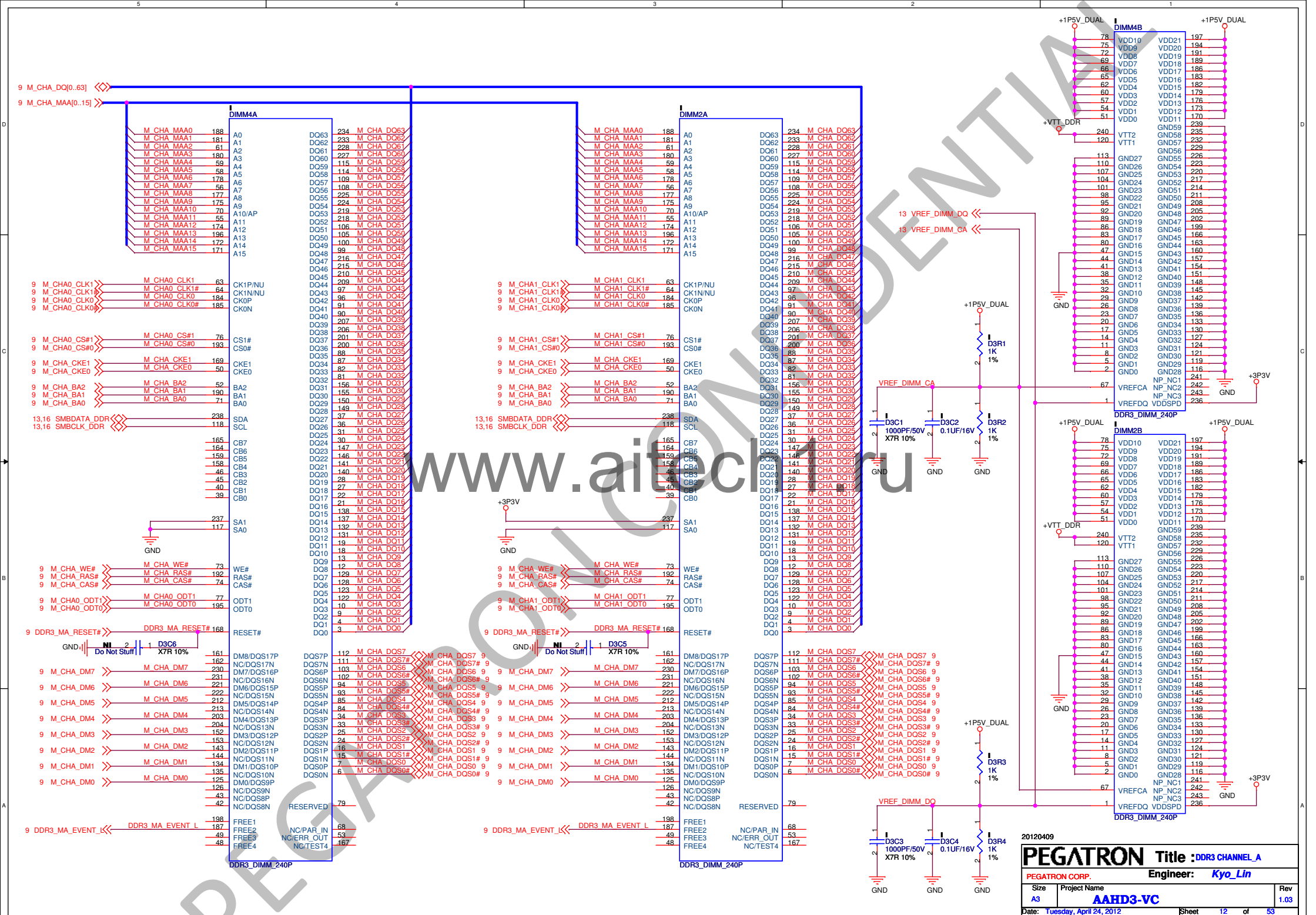


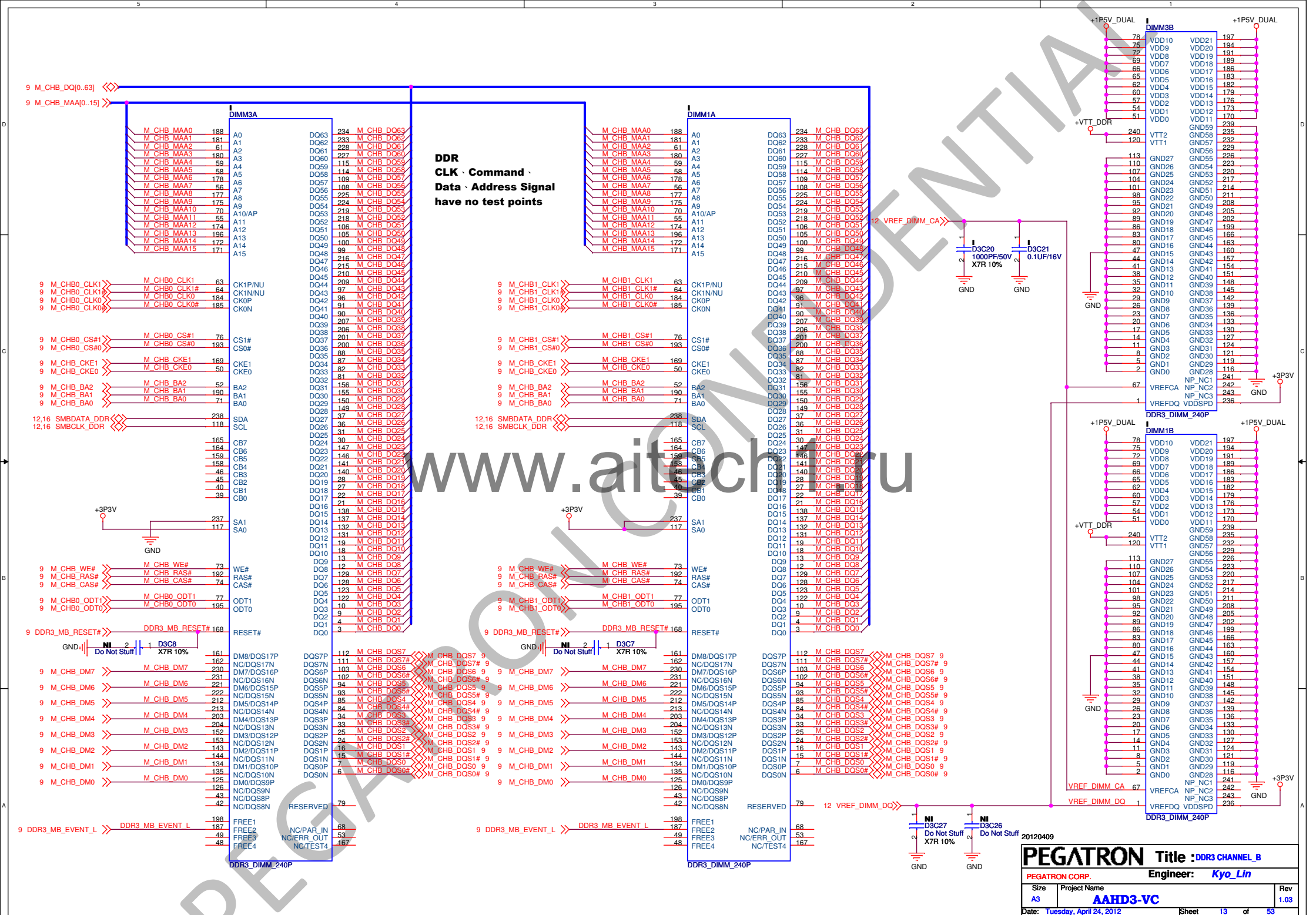
Group A : +VDDA / +VDDIO

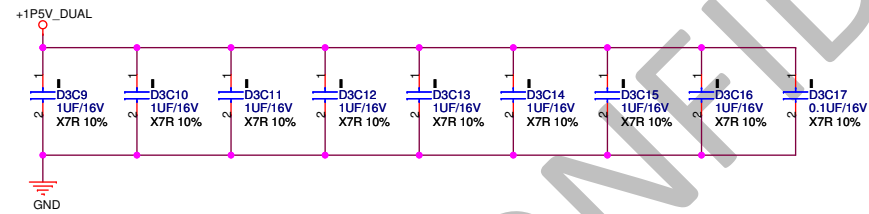
Group B : +VCORE / +VDDNB / +VDDP / +VDDR



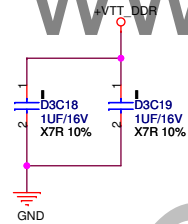






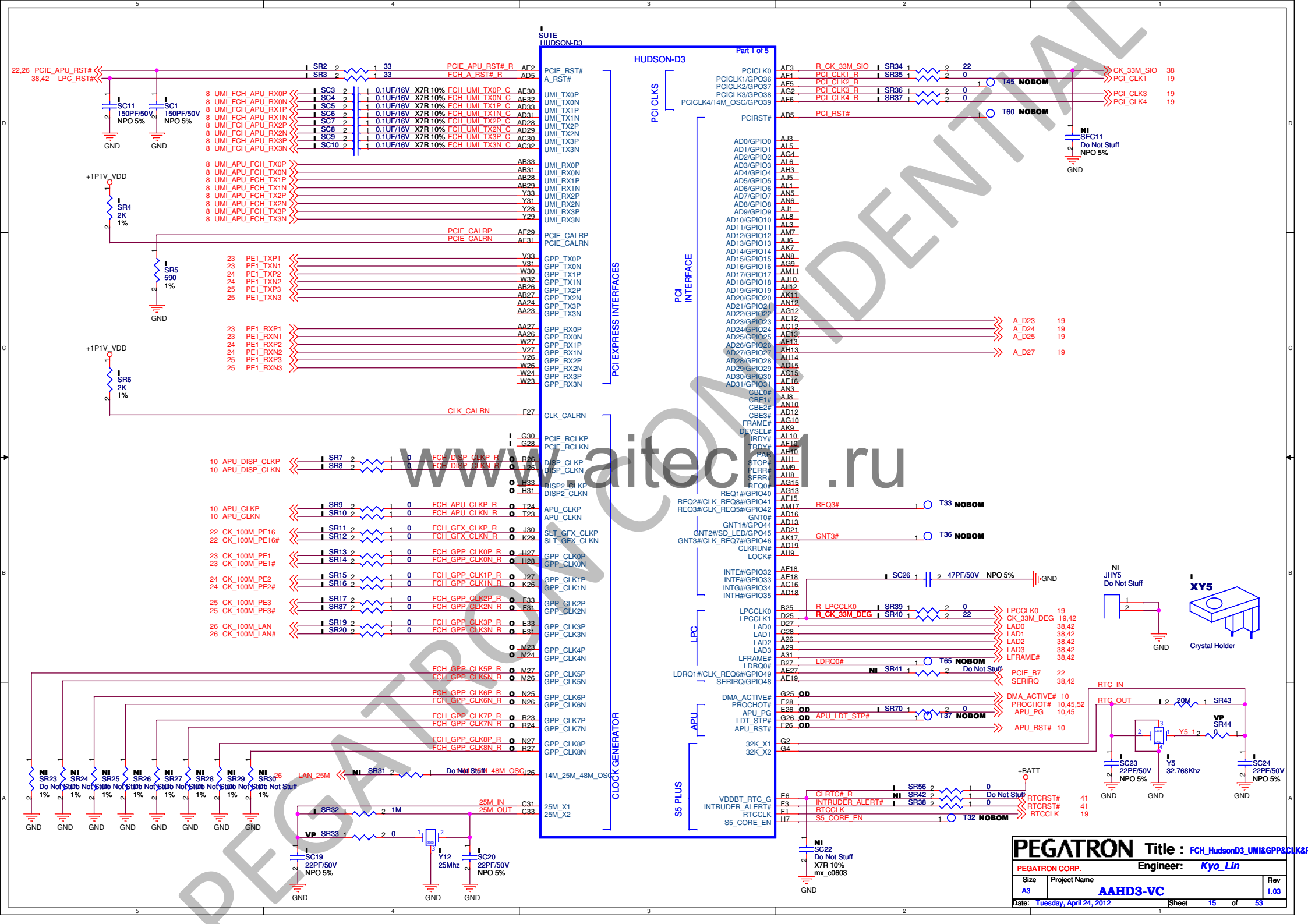


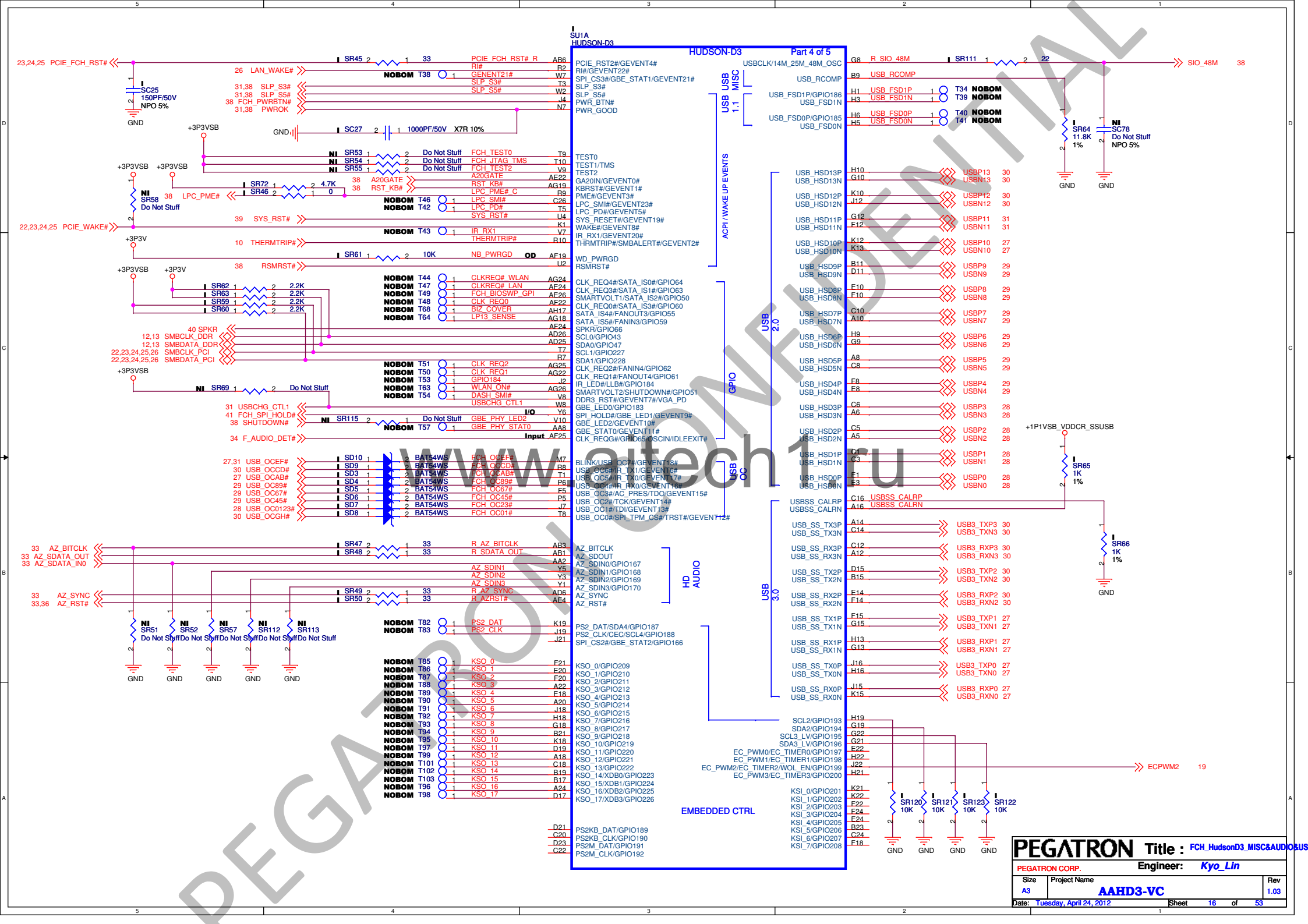
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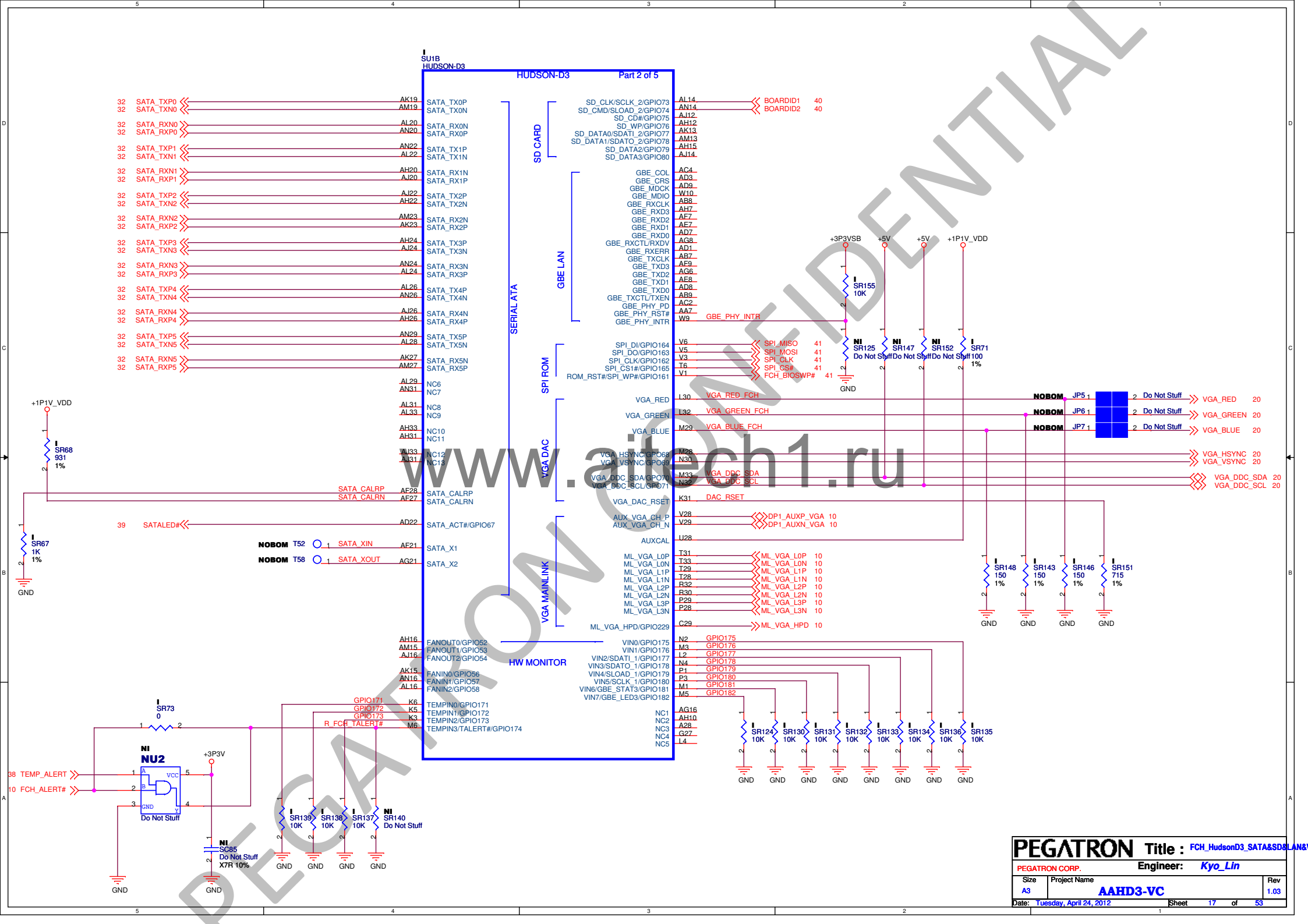


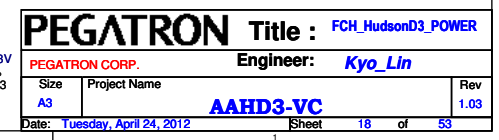
20120409

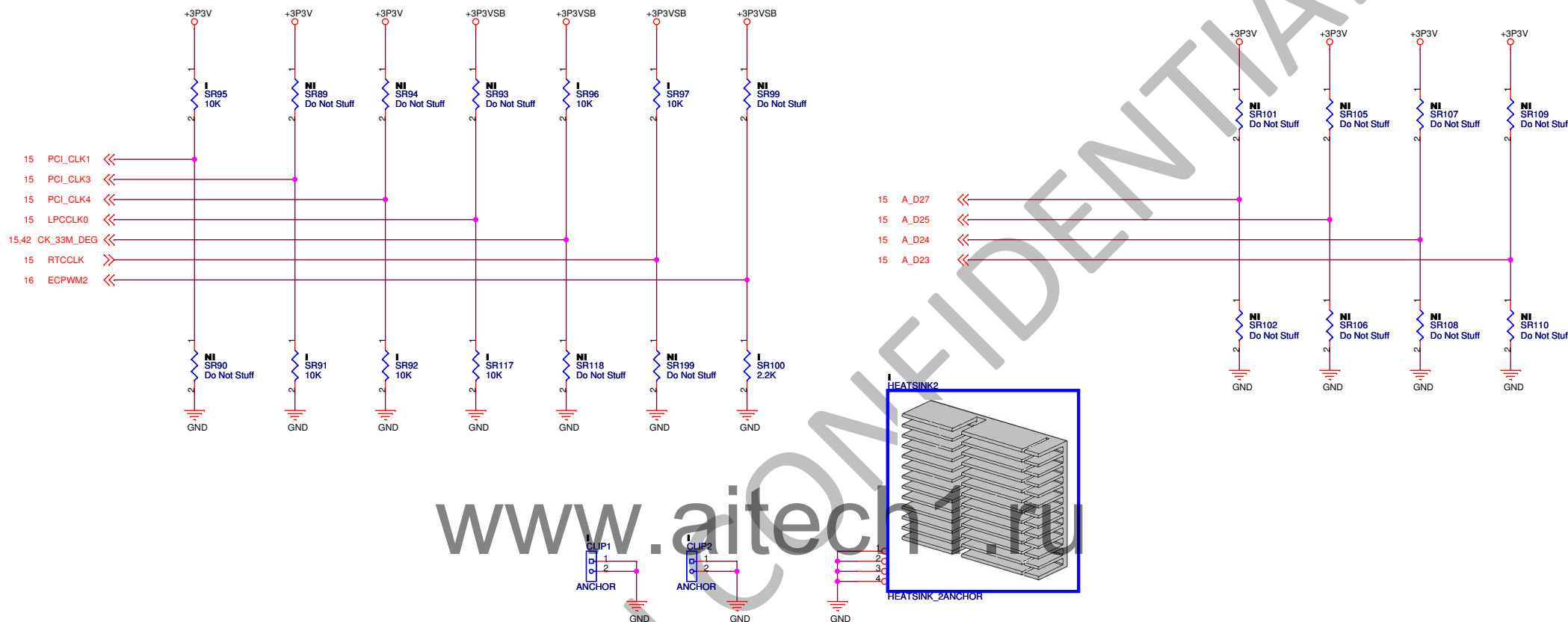
PEGATRON		Title :DDR3 DECOUPLING CAP	
PEGATRON CORP.		Engineer: Kyo_Lin	
Size	Project Name	Rev	
A3	AAHD3-VC	1.03	
Date: Tuesday, April 24, 2012		Sheet 14 of 53	



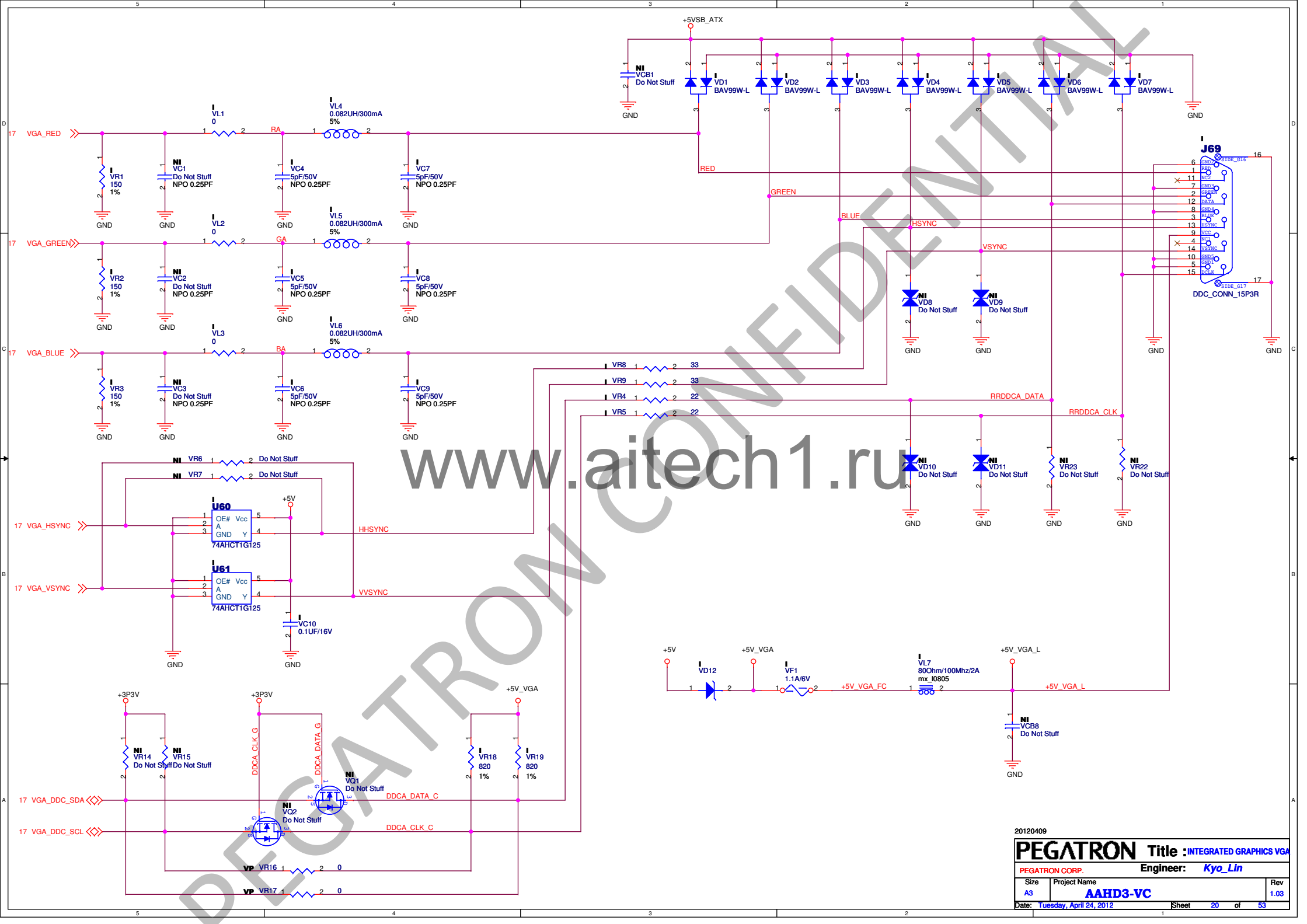








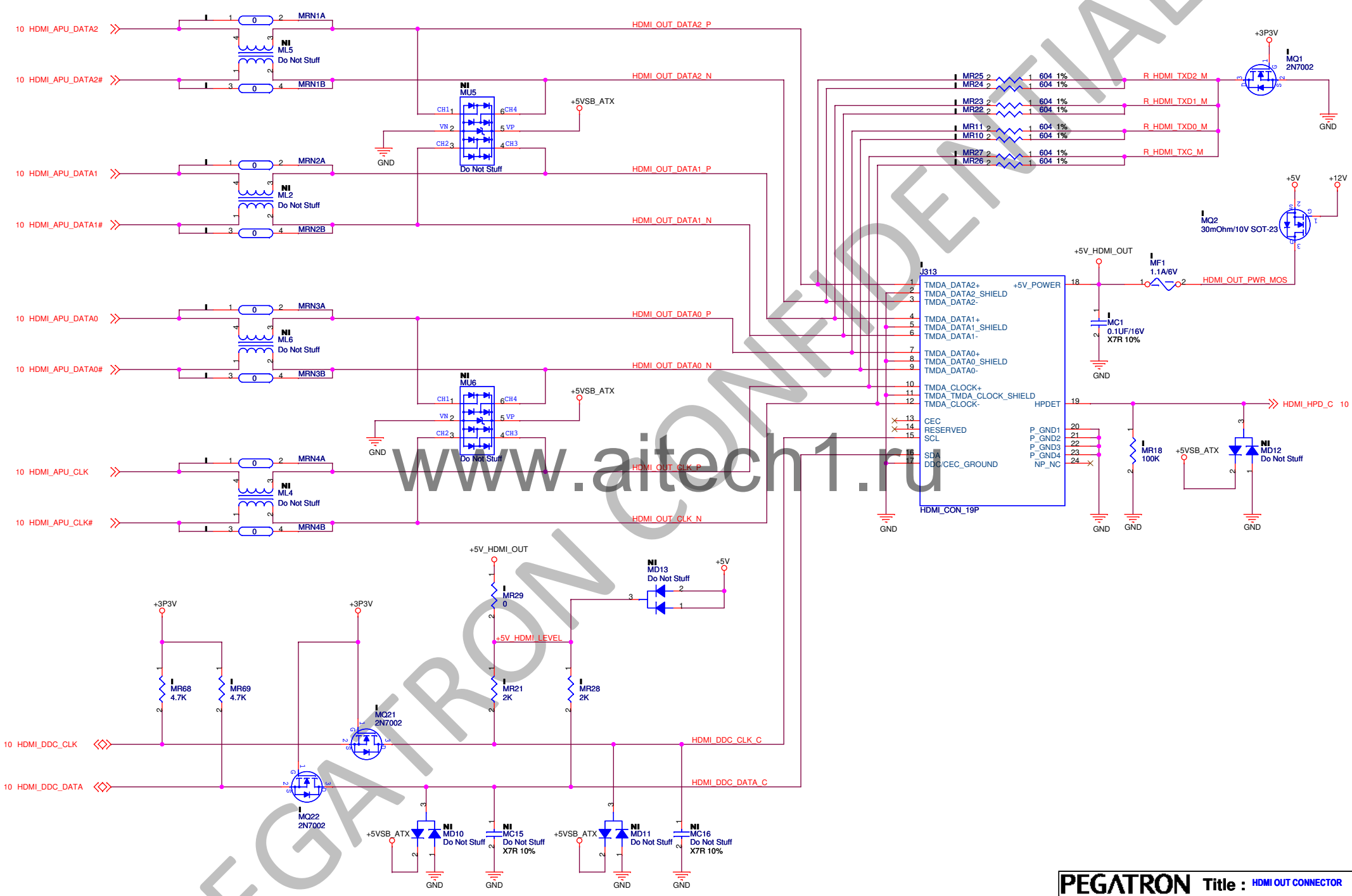
	EC_PWM2 ECPWM2	LPCCLK0 LPCCLK0	LPCCLK1 CK_33M_DEG	PCICLK1 PCI_CLK1	PCICLK3 PCI_CLK3	PCICLK4 PCI_CLK4	RTCCLK RTCCLK
PULL HIGH	LPC ROM	ENABLE IMC	ENABLE INTERNAL CLOCK GENERATOR	ALLOW PCIE GEN2	ENABLE DEBUG MODE	INTER CLOCK REQUIRED SETTING	DISABLE S5+ MODE
PULL LOW	SPI ROM	DISABLE IMC	DISABLE INTERNAL CLOCK GENERATOR	FORCE PCIE GEN2	DISABLE DEBUG MODE	RESERVED	ENABLE S5+ MODE

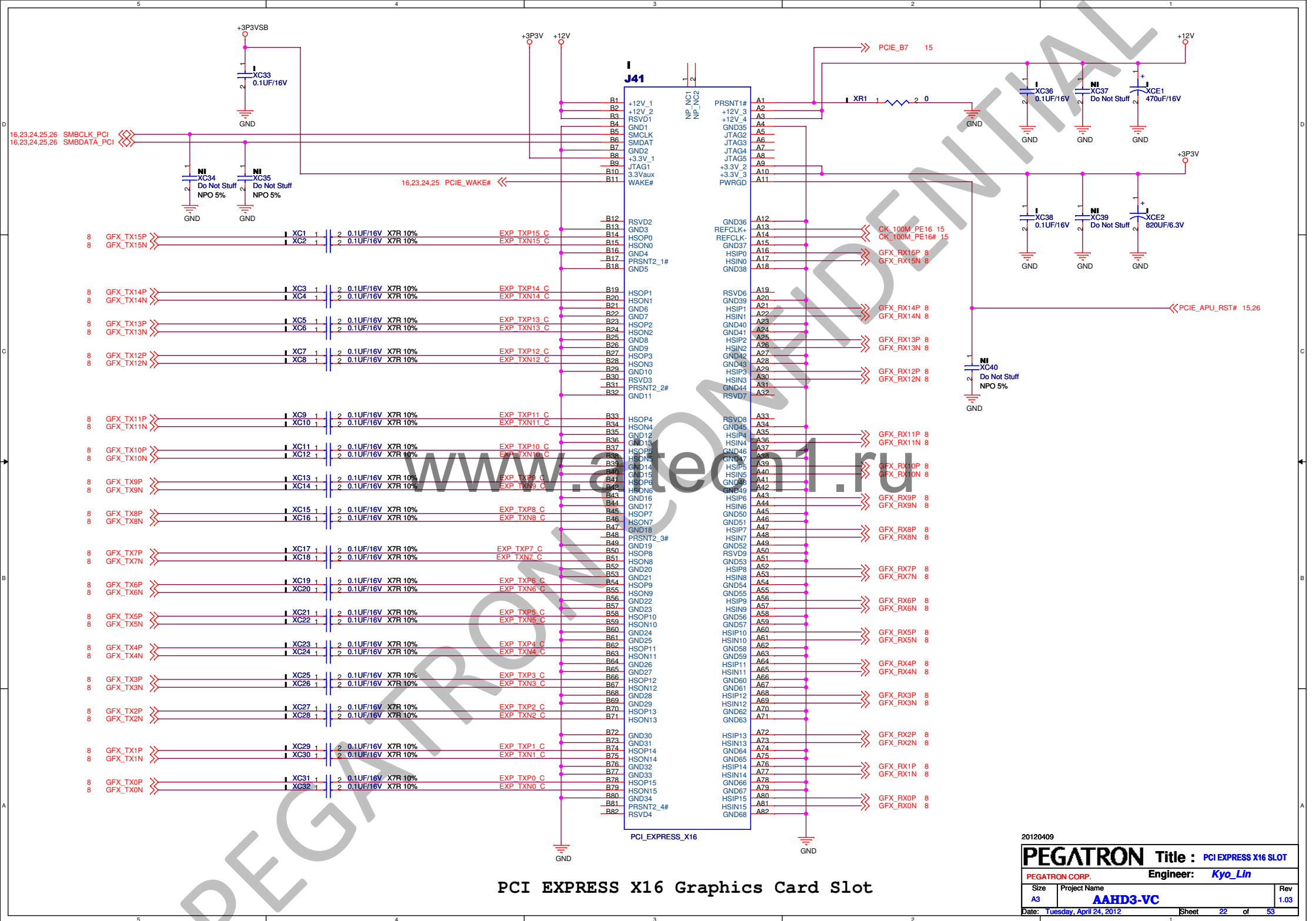


20120409

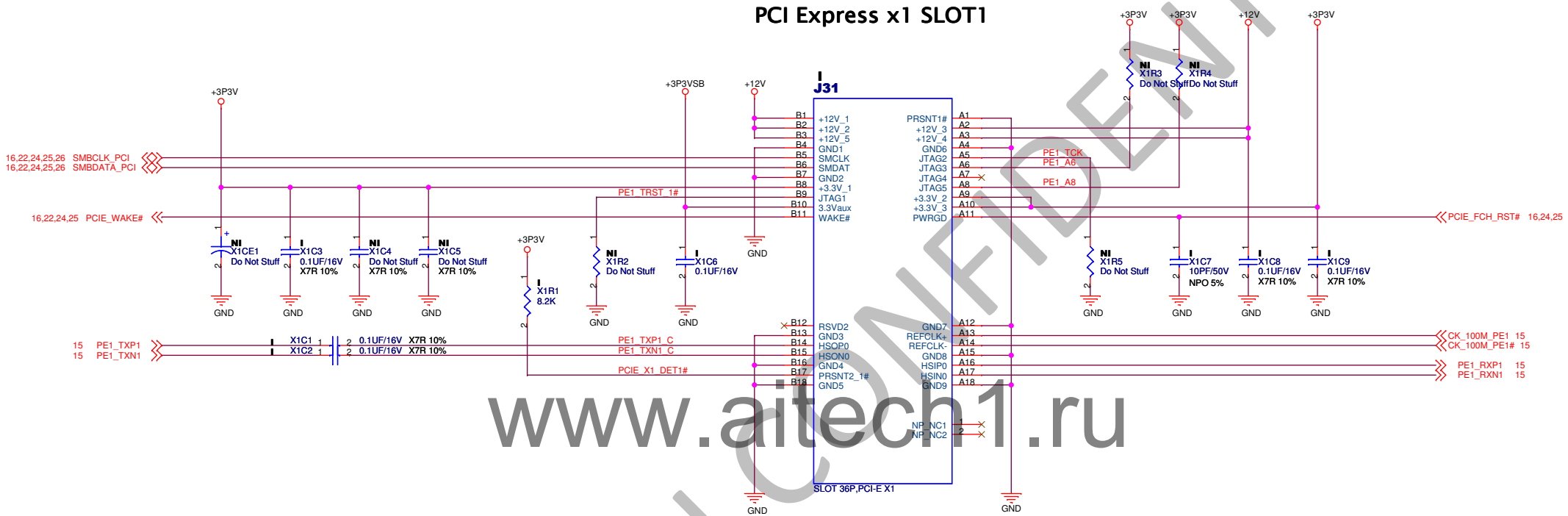
PEGATRON Title : INTEGRATED GRAPHICS VGA
PEGATRON CORP. Engineer: Kyo_Lin

Size	Project Name	Rev
A3	AAHD3-VC	1.03
Date: Tuesday, April 24, 2012		Sheet 20 of 53





PCI Express x1 SLOT1

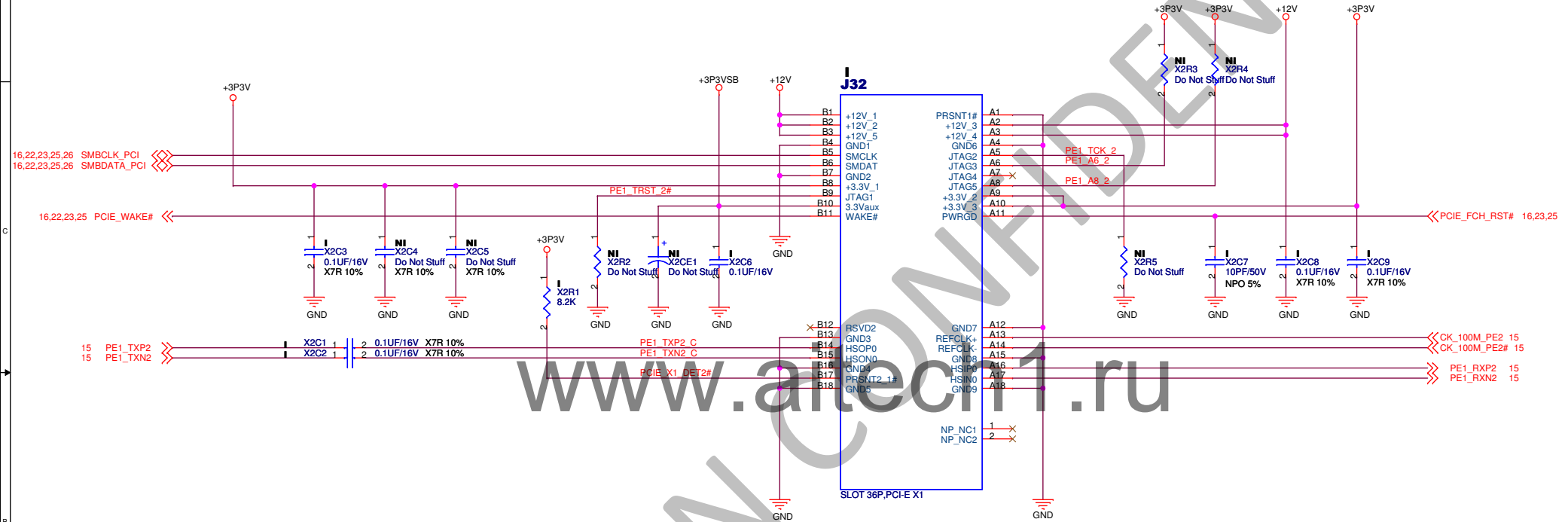


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PEGATRON		Title : PCI EXPRESS X1 SLOT1	
PEGATRON CORP.		Engineer: Kyo_Lin	
Size A3	Project Name AAHD3-VC	Rev 1.03	
Date: Tuesday, April 24, 2012		Sheet 23 of 53	

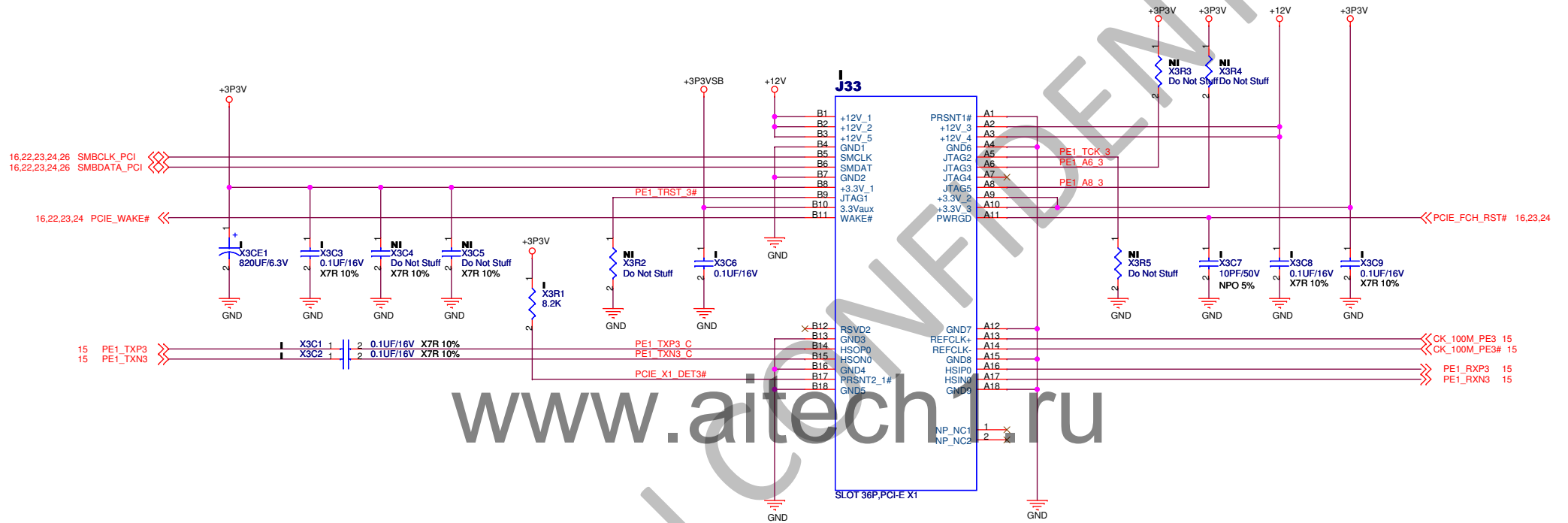
PCI Express x1 SLOT2



20120409

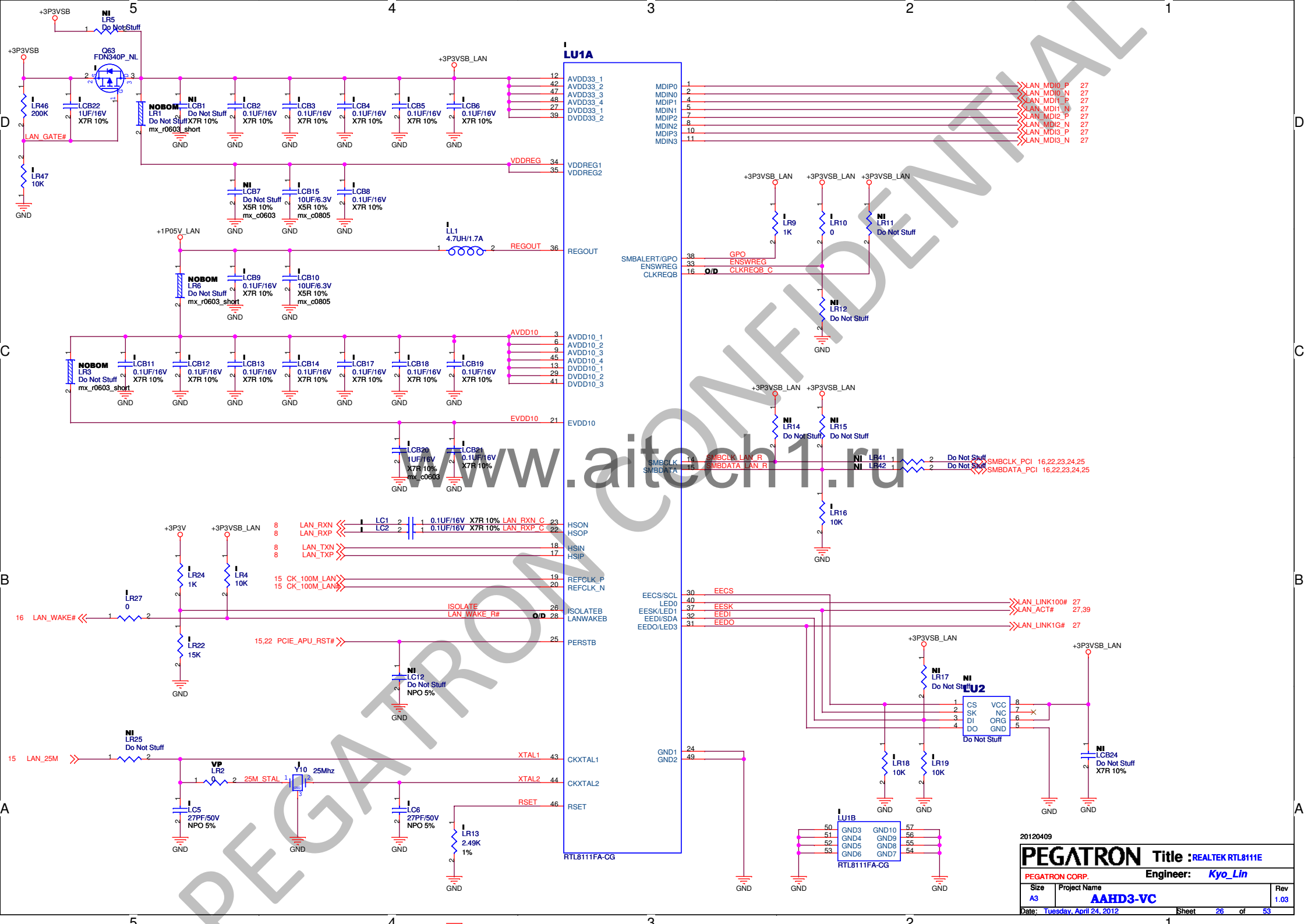
PEGATRON		Title : PCI EXPRESS X1 SLOT2	
PEGATRON CORP.		Engineer: Kyo_Lin	
Size A3	Project Name AAHD3-VC	Rev 1.03	
Date: Tuesday, April 24, 2012		Sheet 24	of 53

PCI Express x1 SLOT3



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PEGATRON		Title : PCI EXPRESS X1 SLOT3	
PEGATRON CORP.		Engineer: Kyo_Lin	
Size	Project Name		Rev
A3	AAHD3-VC		1.03
Date: Tuesday, April 24, 2012		Sheet 25 of 53	



20120409

PEGATRON Title : REALTEK RTL8111E

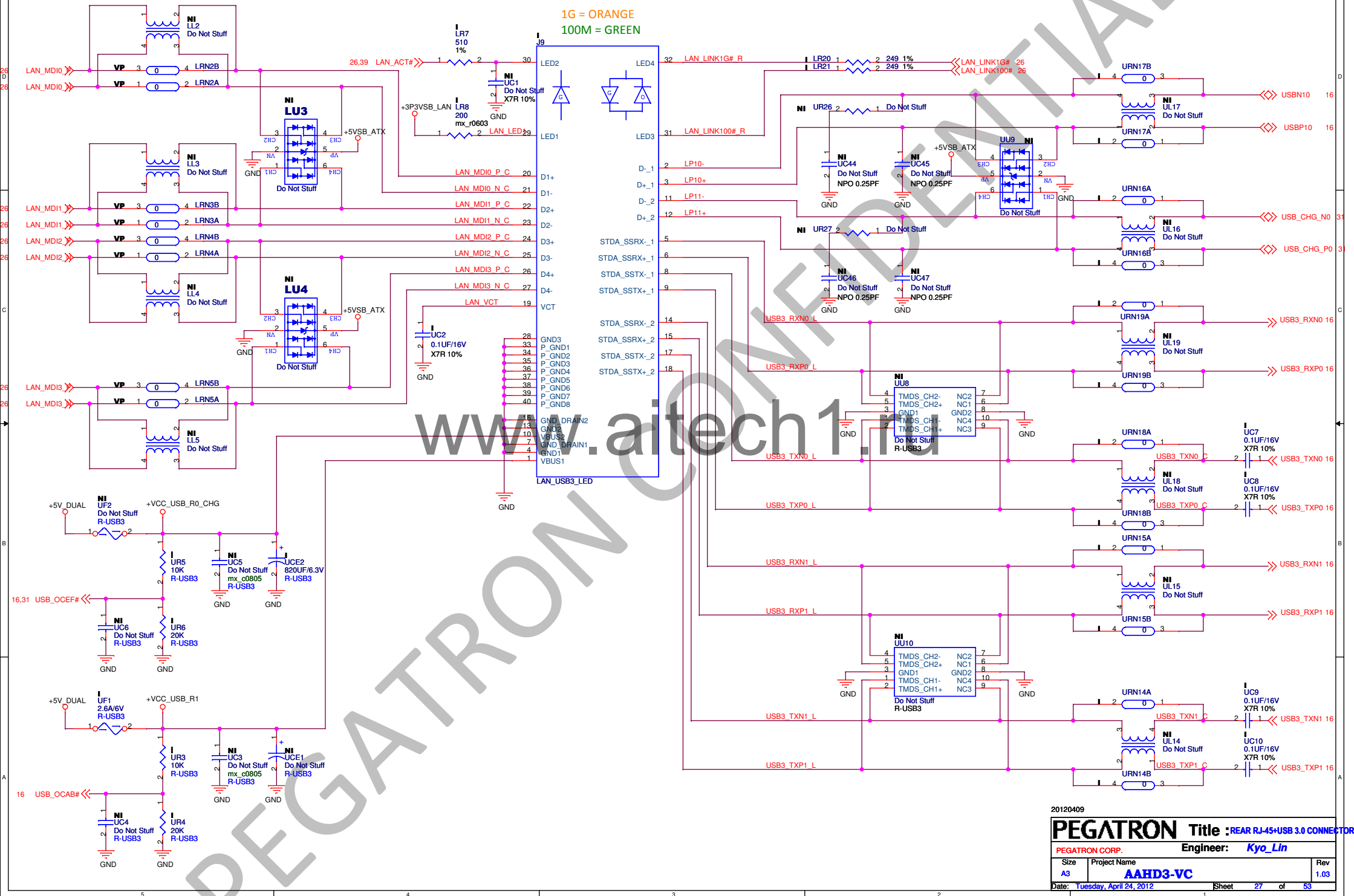
PEGATRON CORP. Engineer: Kyo_Lin

Size A3	Project Name AAHD3-VC	Rev 1.03
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Date: Tuesday, April 24, 2012 Sheet 26 of 53

LAN + Dual USB3.0 CONNECTOR

1G = ORANGE
100M = GREEN



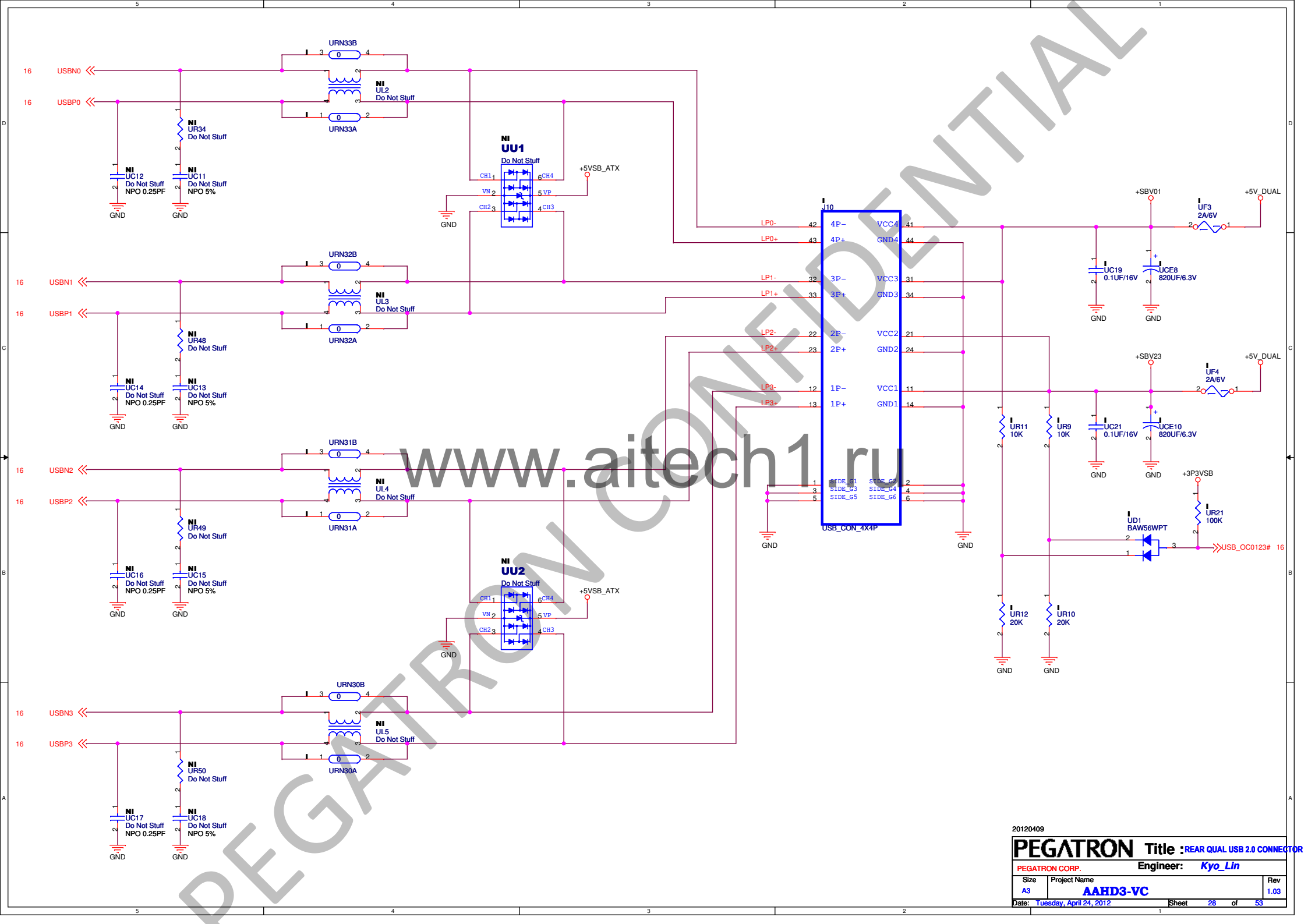
20120409

PEGATRON Title : REAR RJ45+USB 3.0 CONNECTOR

PEGATRON CORP. Engineer: Kyo_Lin

Size A3 Project Name AAHD3-VC

Date: Tuesday, April 24, 2012 Sheet 27 of 53



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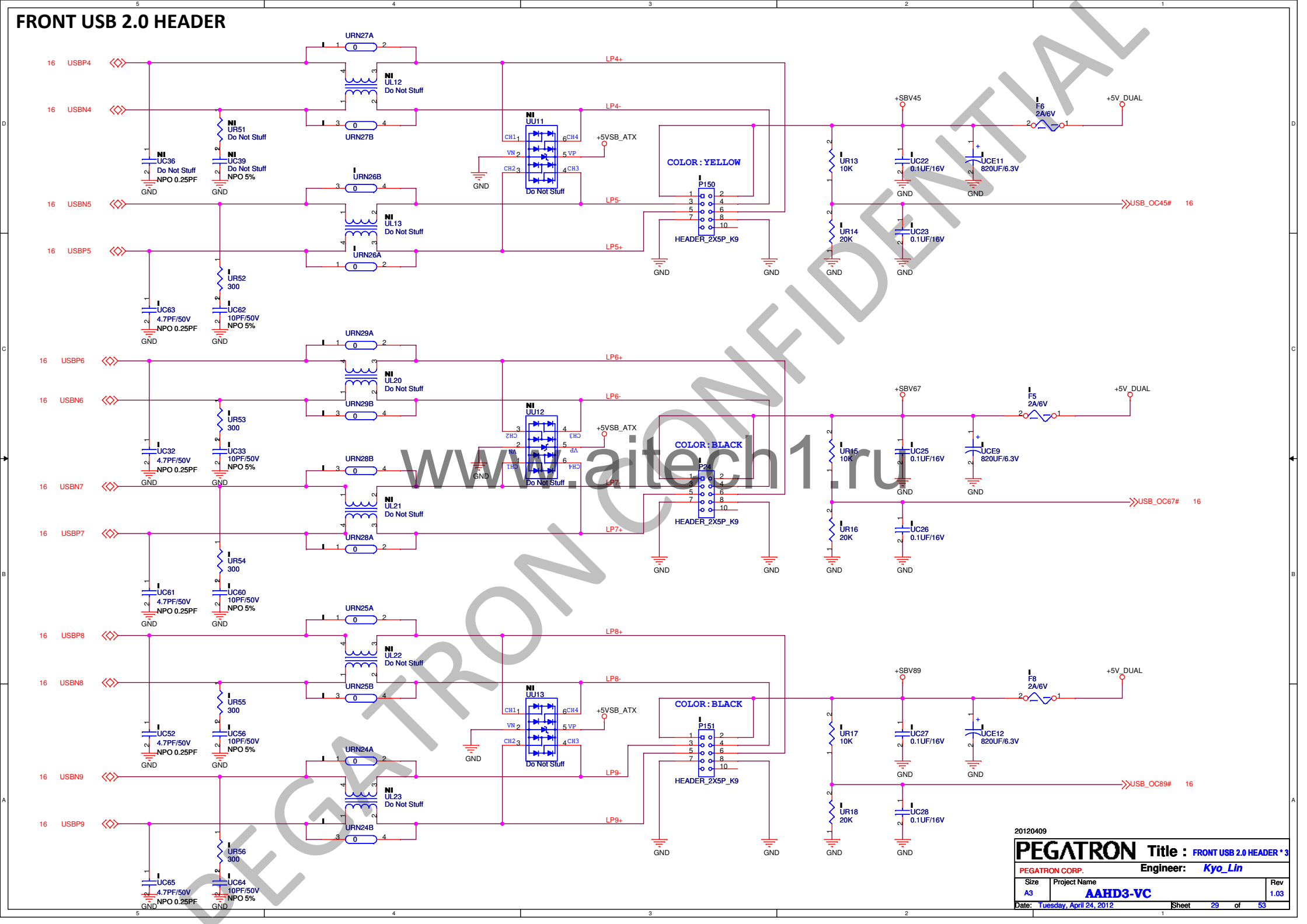
PEGATRON Title : REAR QUAL USB 2.0 CONNECTOR

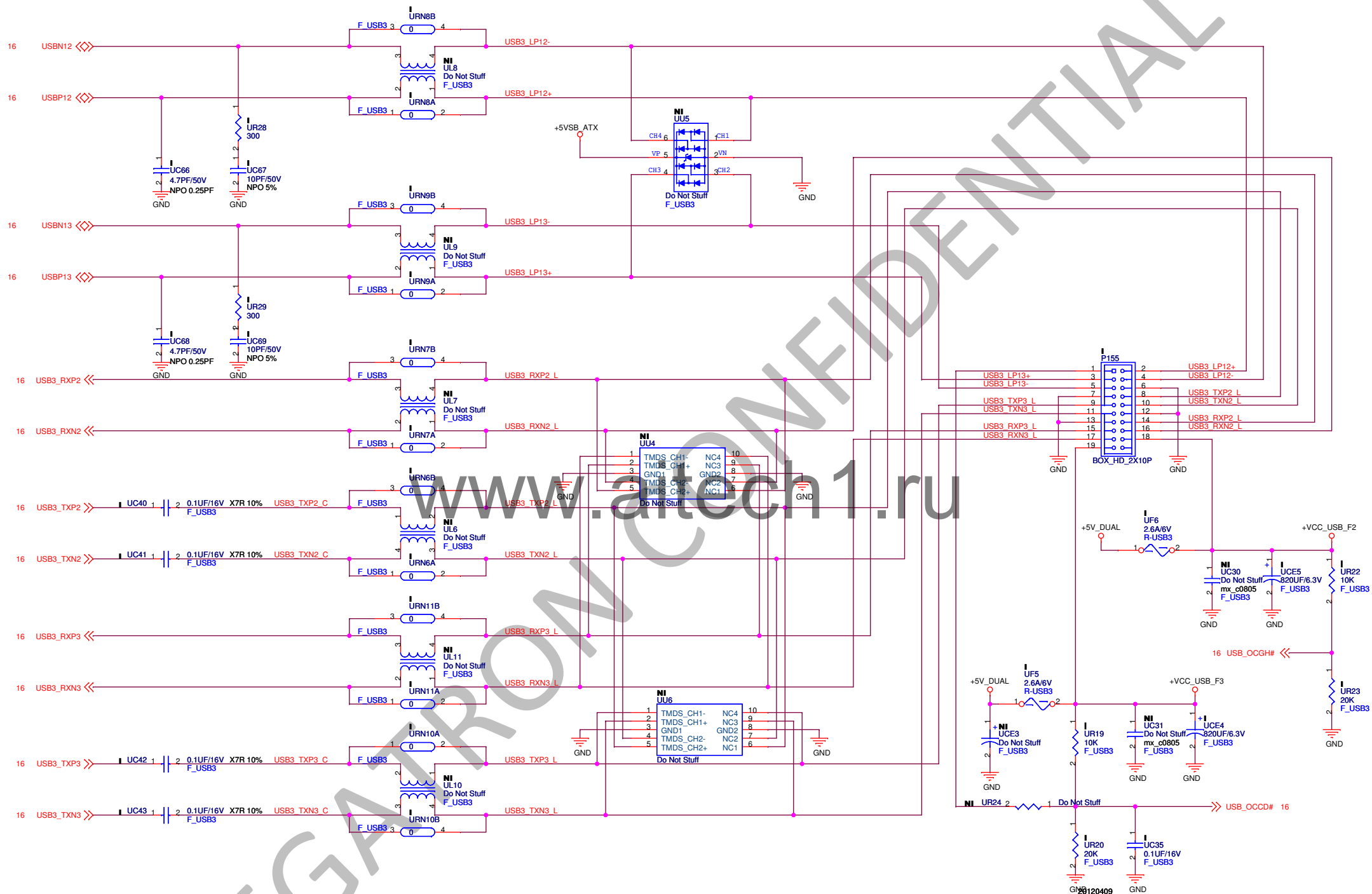
PEGATRON CORP. Engineer: Kyo_Lin

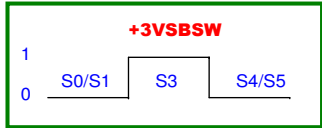
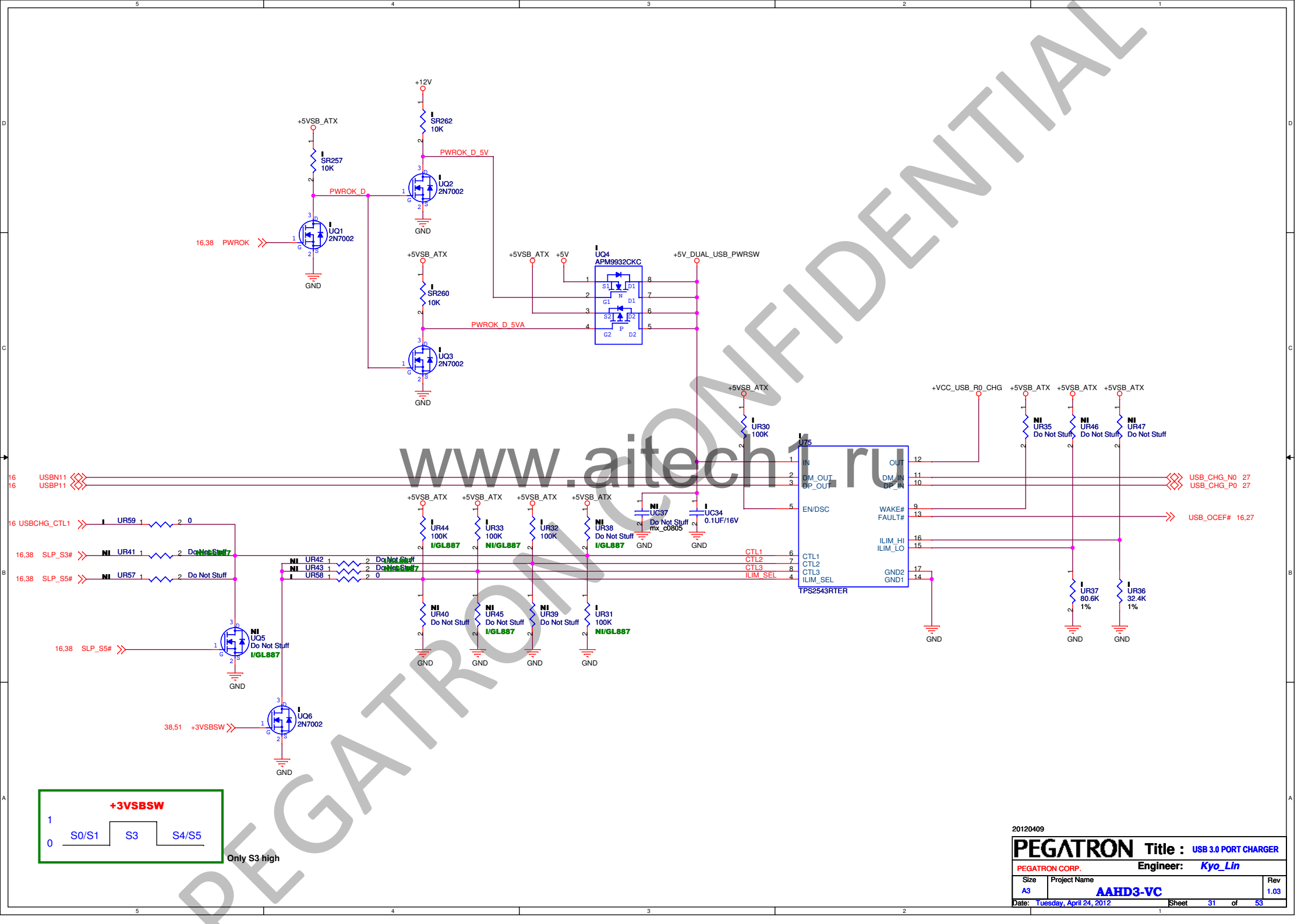
Size A3 Project Name AAHD3-VC Rev 1.03

Date: Tuesday, April 24, 2012 Sheet 28 of 53

FRONT USB 2.0 HEADER

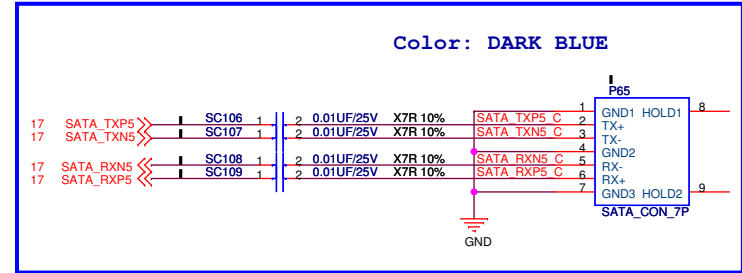
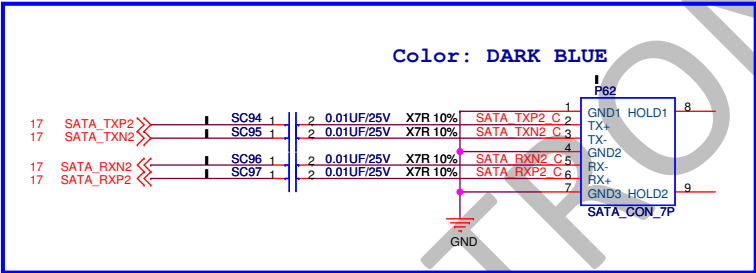
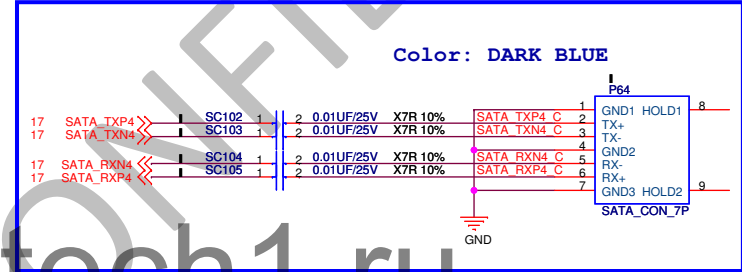
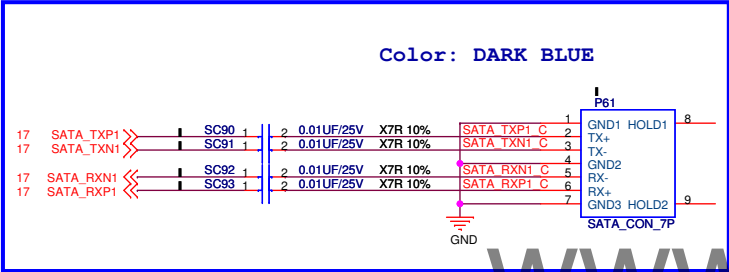
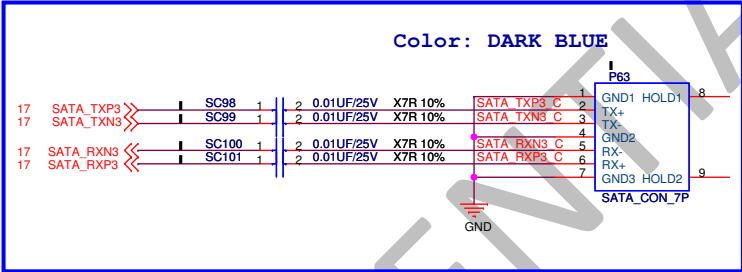
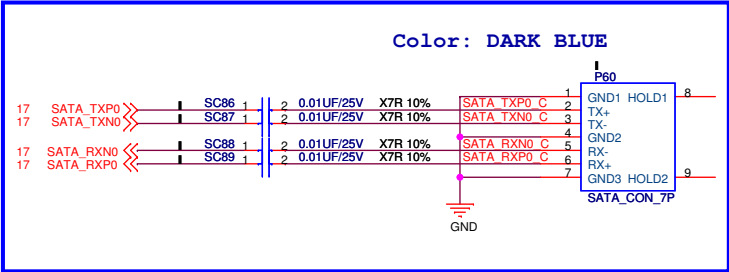


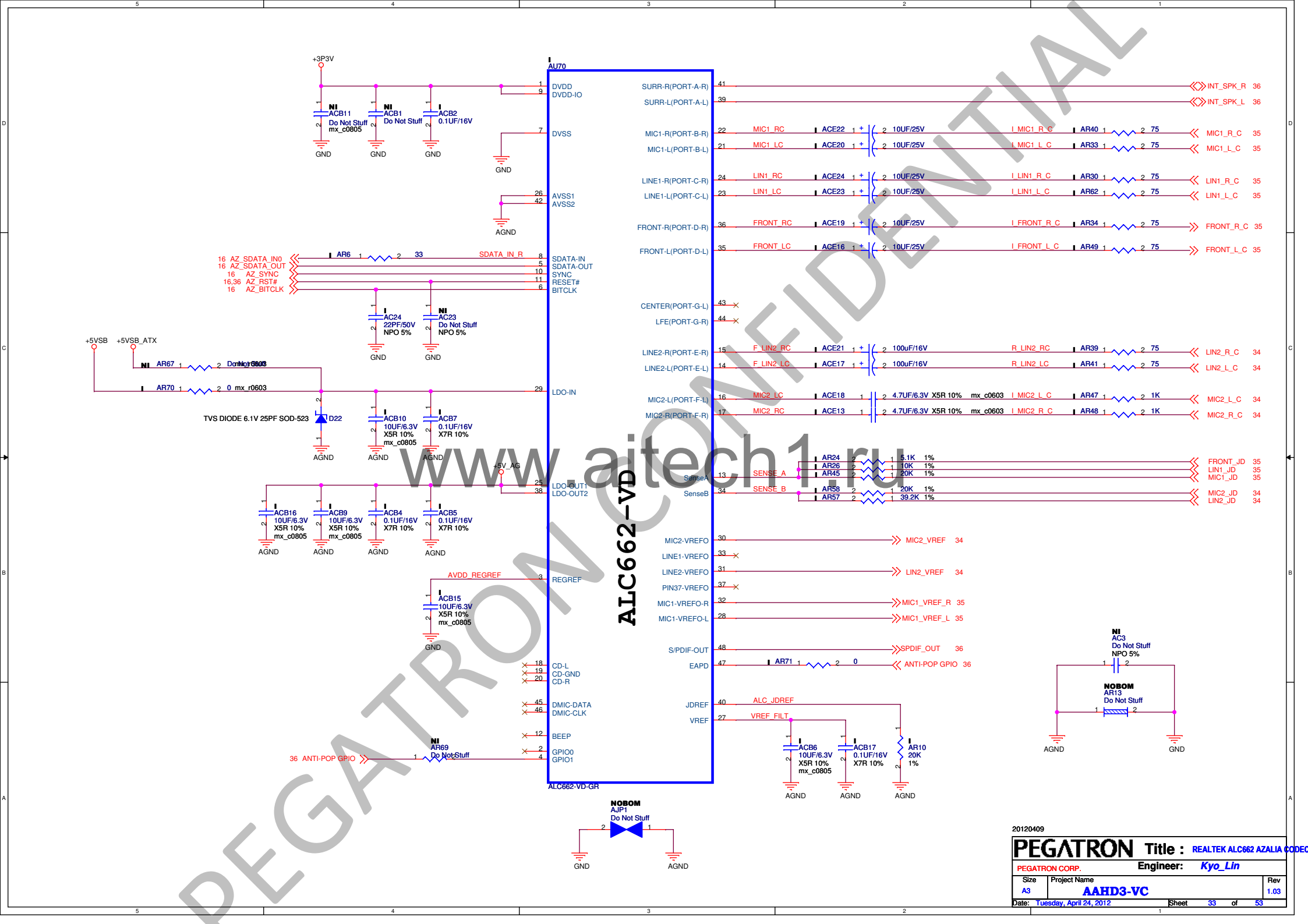




Only S3 high

SERIAL ATA CONNECTOR





20120409

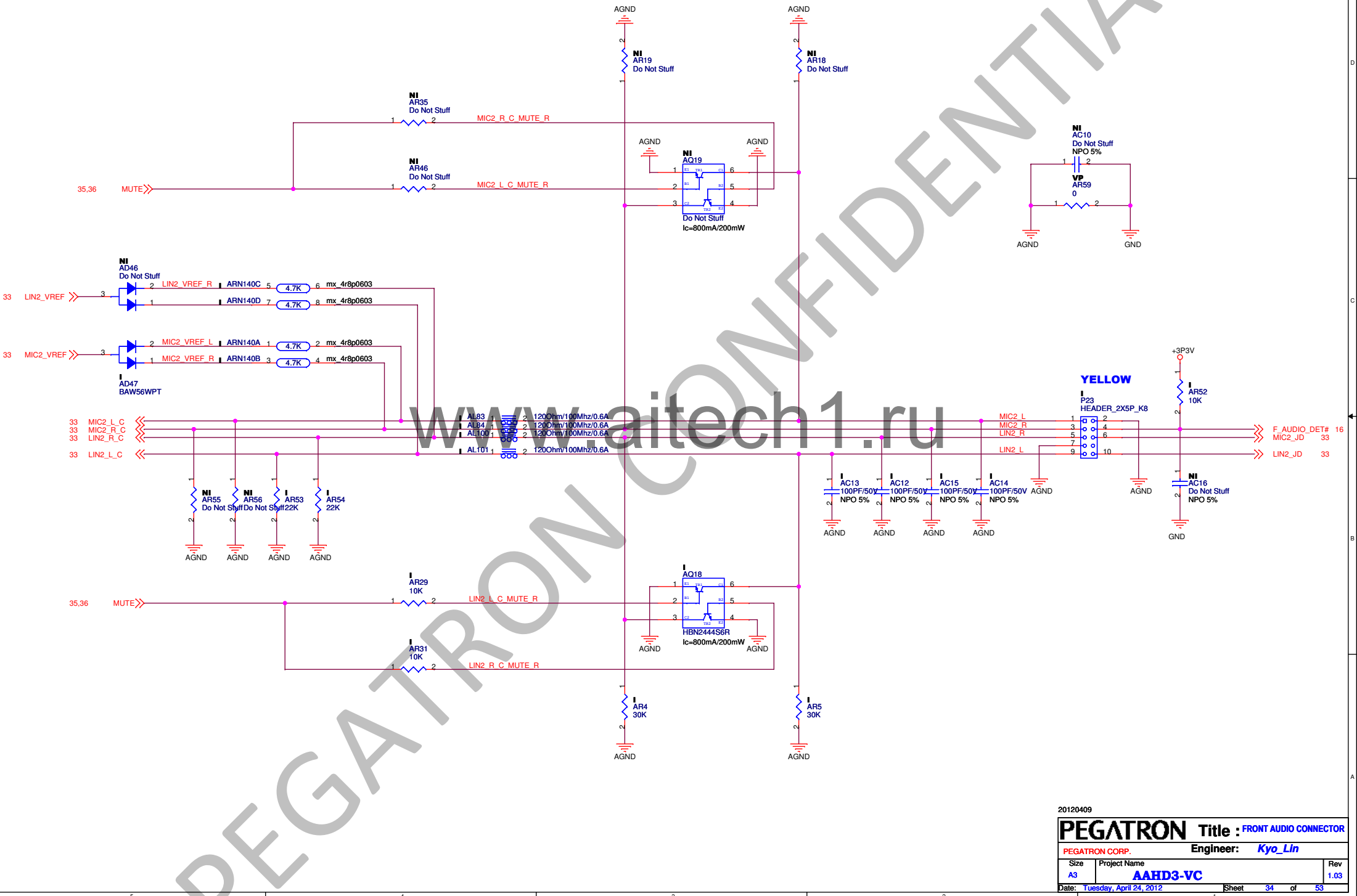
PEGATRON Title : REALTEK ALC662 AZALIA CODE

PEGATRON CORP. Engineer: Kyo_Lin

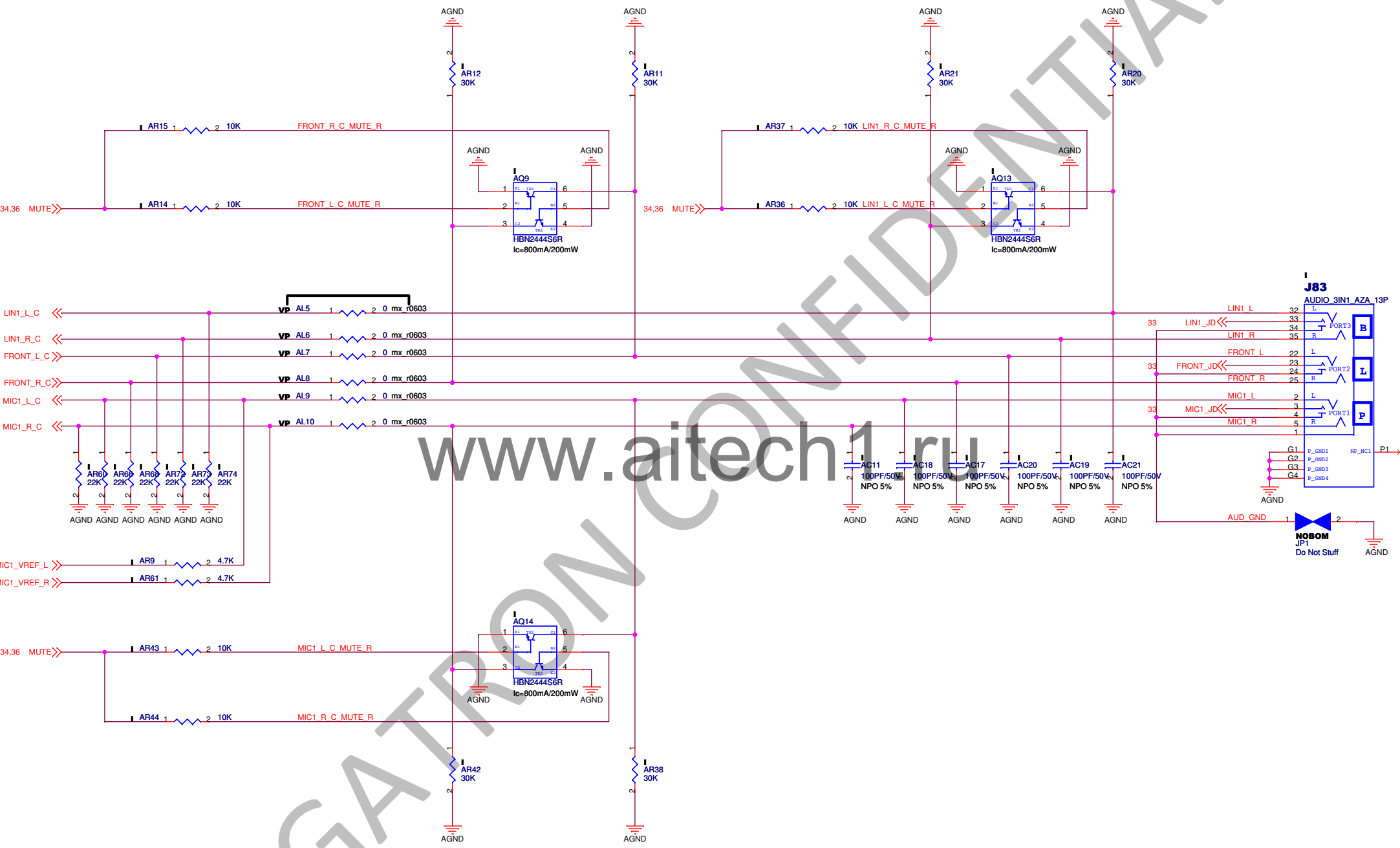
Size A3 Project Name AAHD3-VC Rev 1.03

Date: Tuesday, April 24, 2012 Sheet 33 of 53

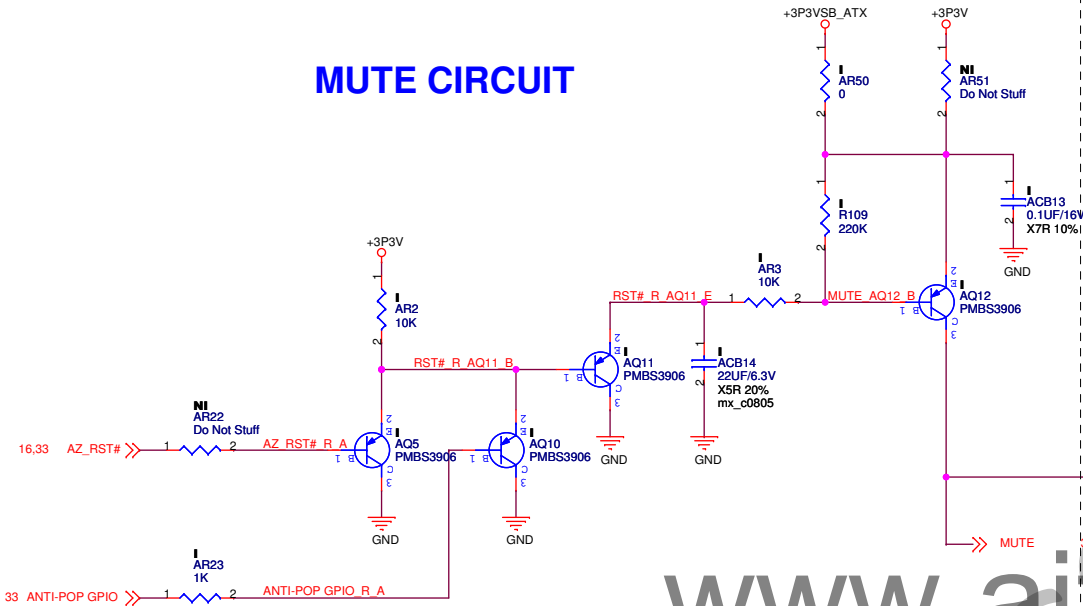
Front Audio Header



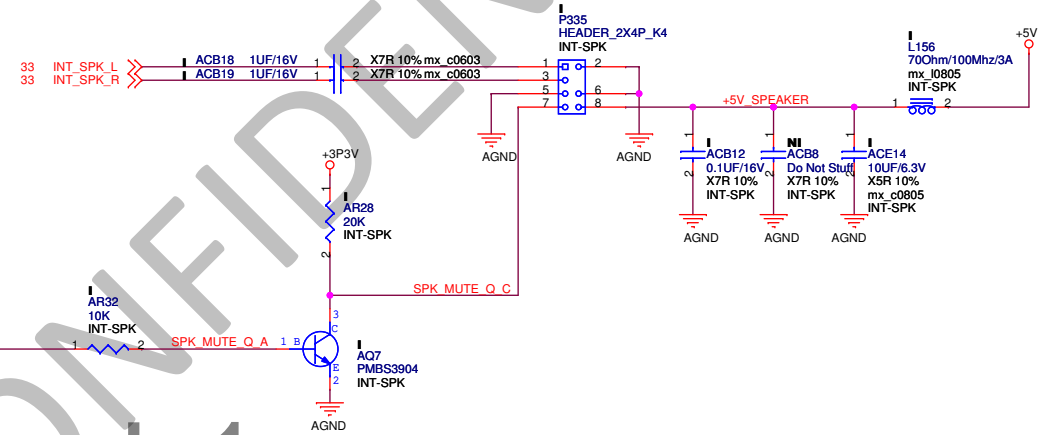
Azalia Rear Audio Connector



MUTE CIRCUIT

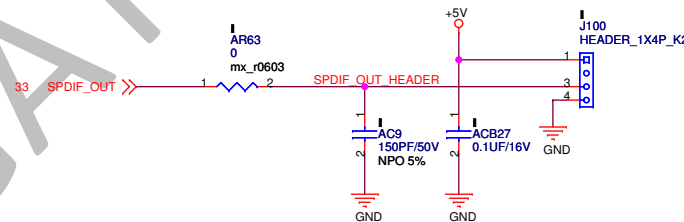


INT-SPK



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SPDIF OUT



20120409

PEGATRON Title :INT-SPK & SPDIF OUT HEADER

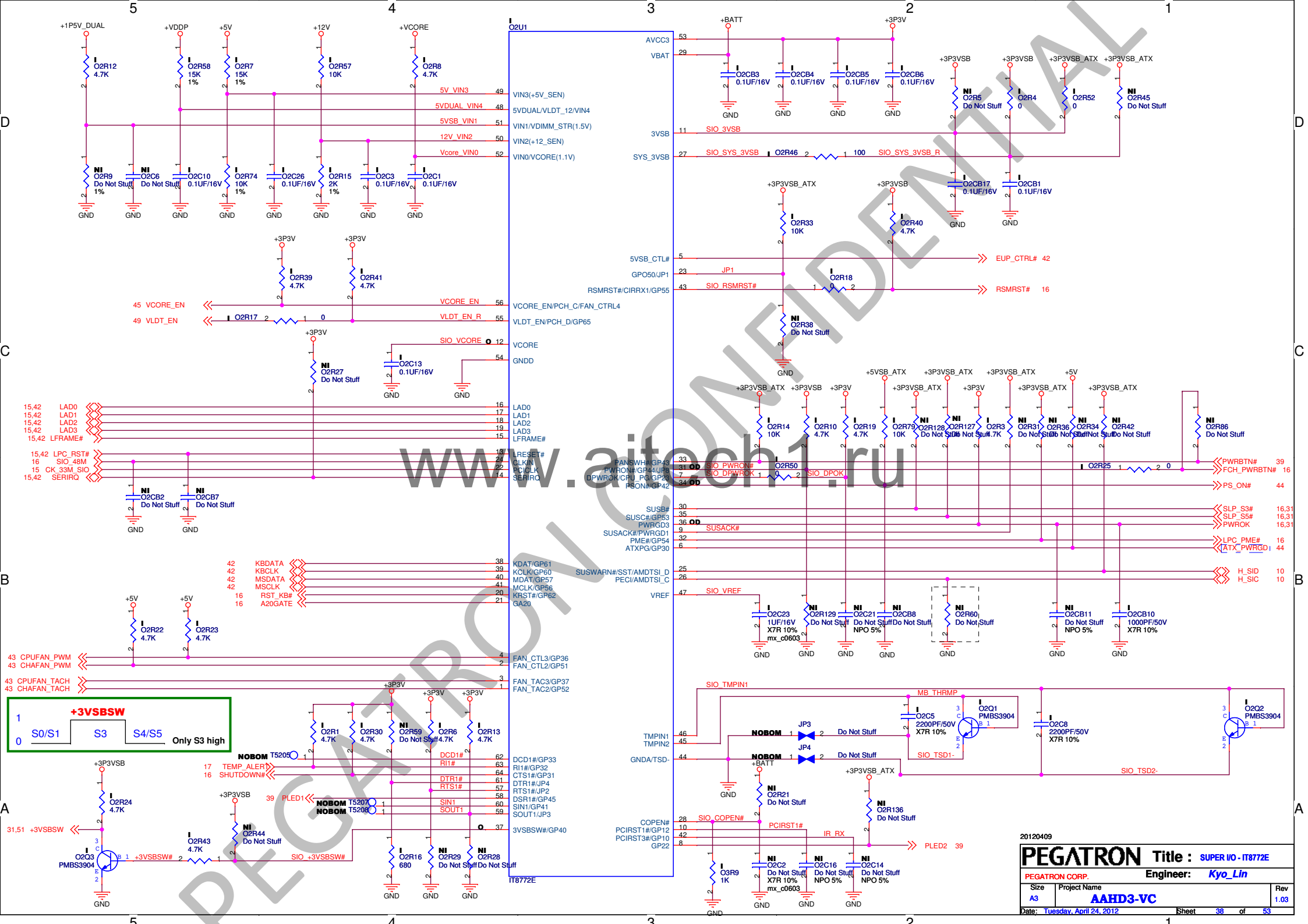
PEGATRON CORP. Engineer: Kyo_Lin

Size A3 Project Name AAHD3-VC Rev 1.03

Date: Tuesday, April 24, 2012 Sheet 36 of 53

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20120409		Title :COM PORT	
PEGATRON CORP.		Engineer: Kyo_Lin	
Size	Project Name	Rev	
A3	AAHD3-VC	1.03	
Date: Monday, March 19, 2012		Sheet	37 of 53



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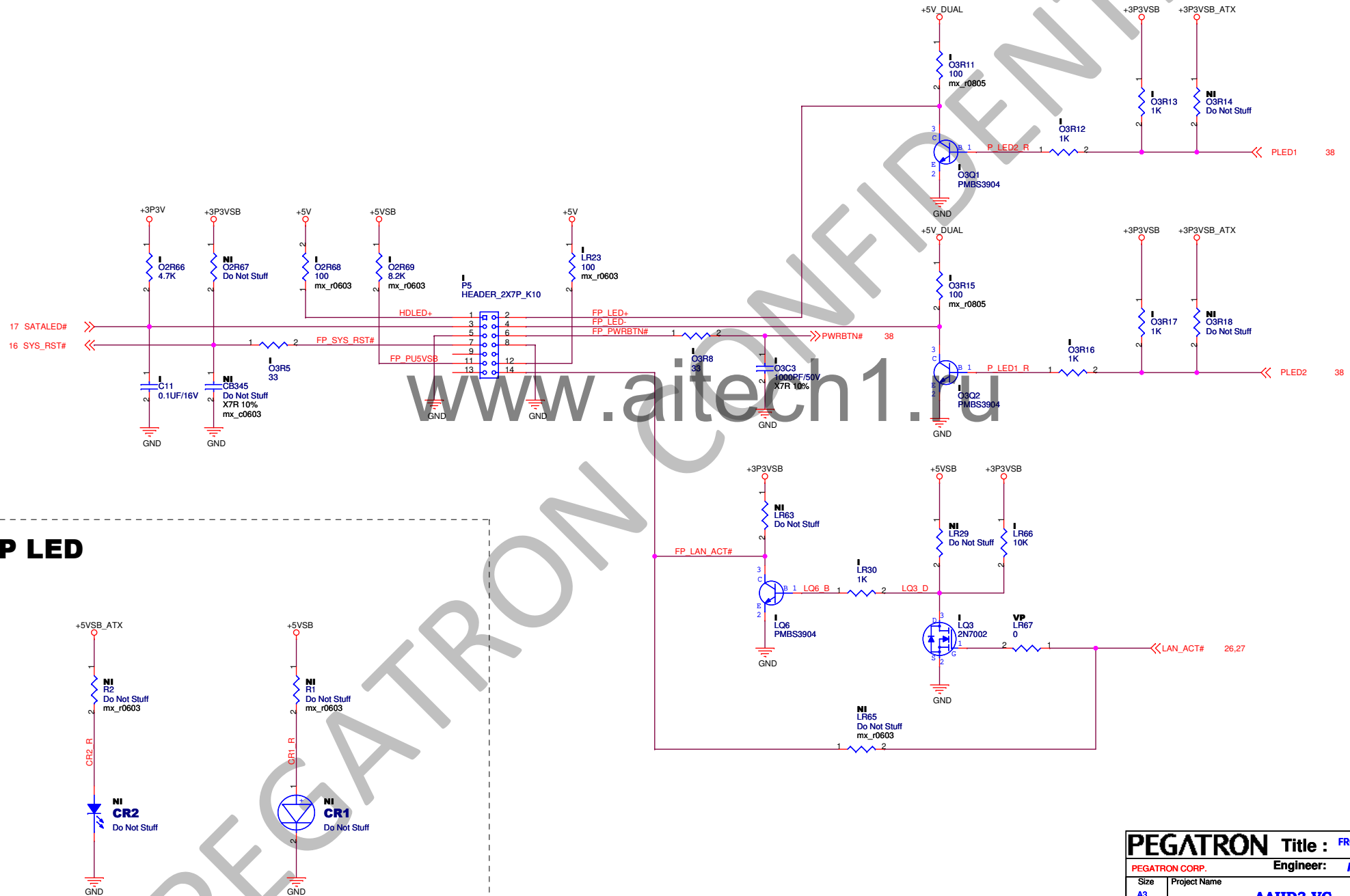
PEGATRON Title : SUPER VO - IT8772E

PEGATRON CORP. Engineer: Kyo_Lin

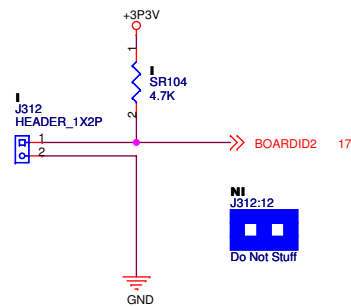
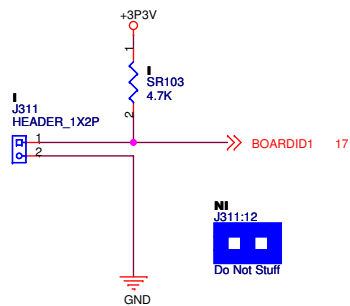
Size A3 Project Name AAHD3-VC

Date: Tuesday, April 24, 2012 Sheet 38 of 53

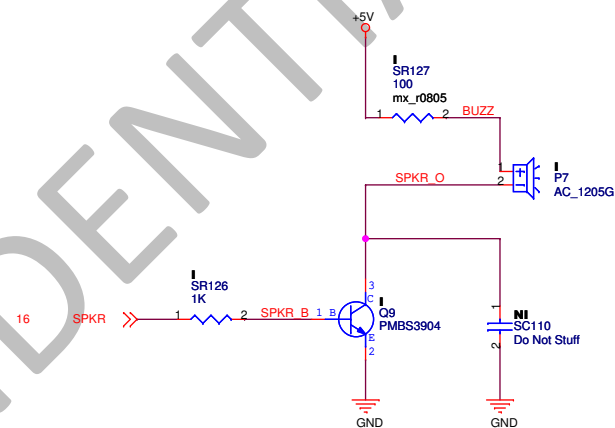
HPD CONTROL PANEL / LED CIRCUITRY



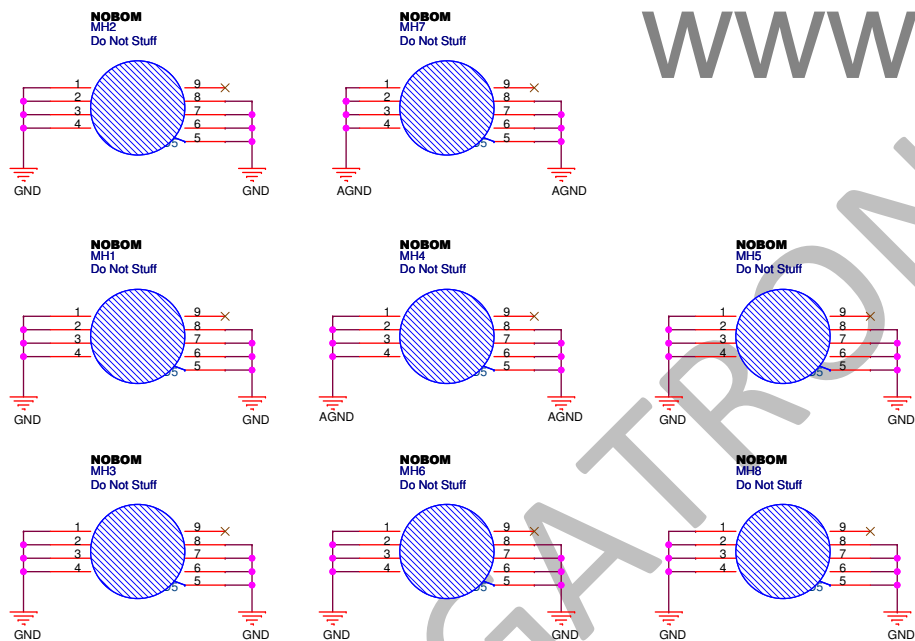
BOARD ID SELECT



BUZZER



ONLY FOR SCREW HOLE



PCB1
PCB BOARD
uATX-PCB
9.6" X 9.6"

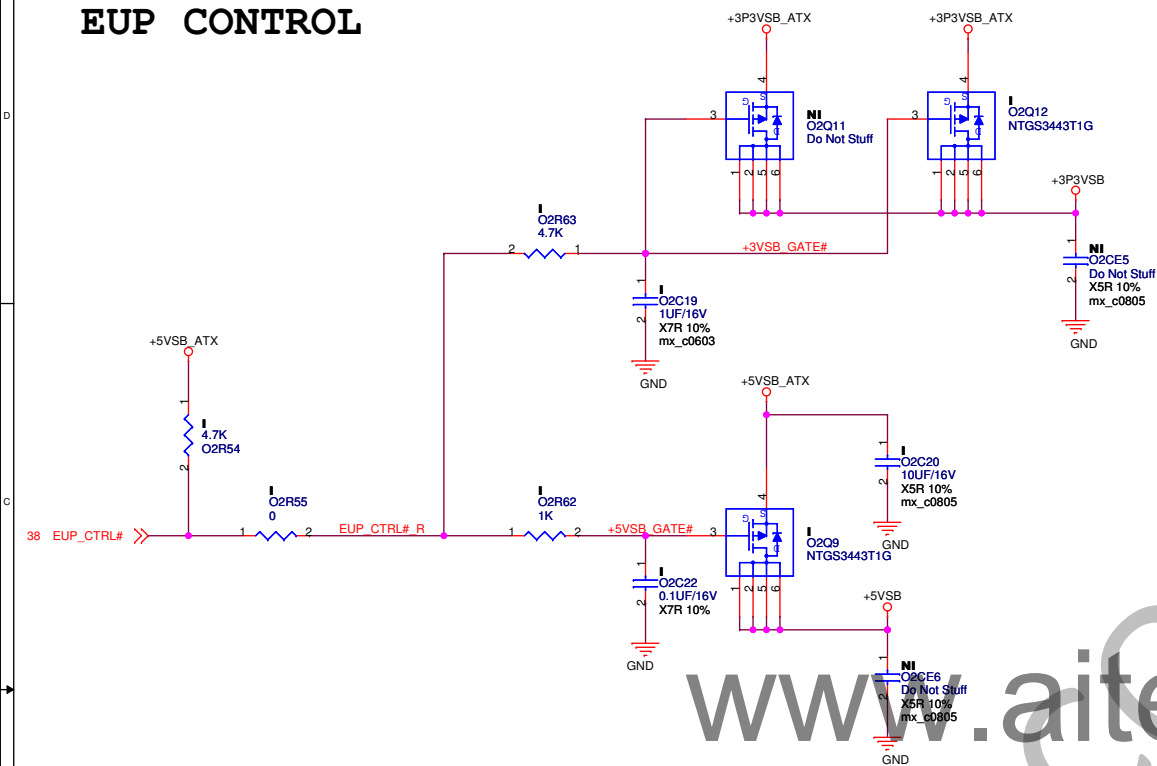
LABEL1
PCB LABEL
PPID LABEL

LABEL2
PCB LABEL
BIOS
LABEL

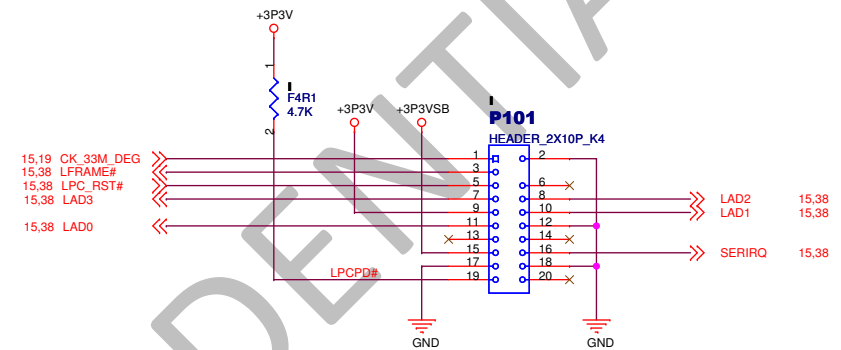
LABEL3
PCB LABEL
BLANK
SN
LABEL

20120409

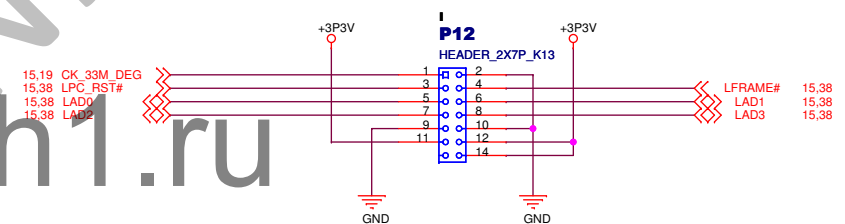
EUP CONTROL



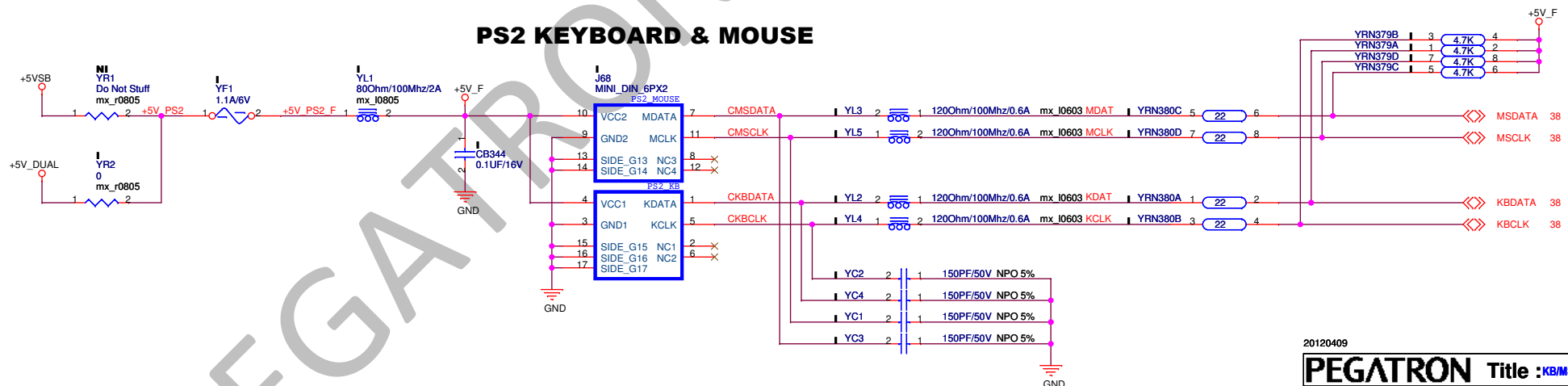
TPM HEADER



LPC DEBUG

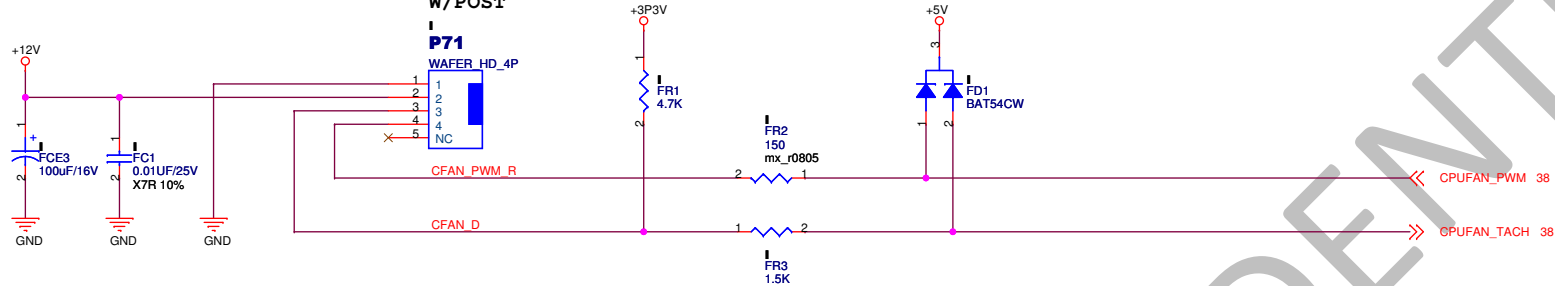


PS2 KEYBOARD & MOUSE



CPU FAN Connector

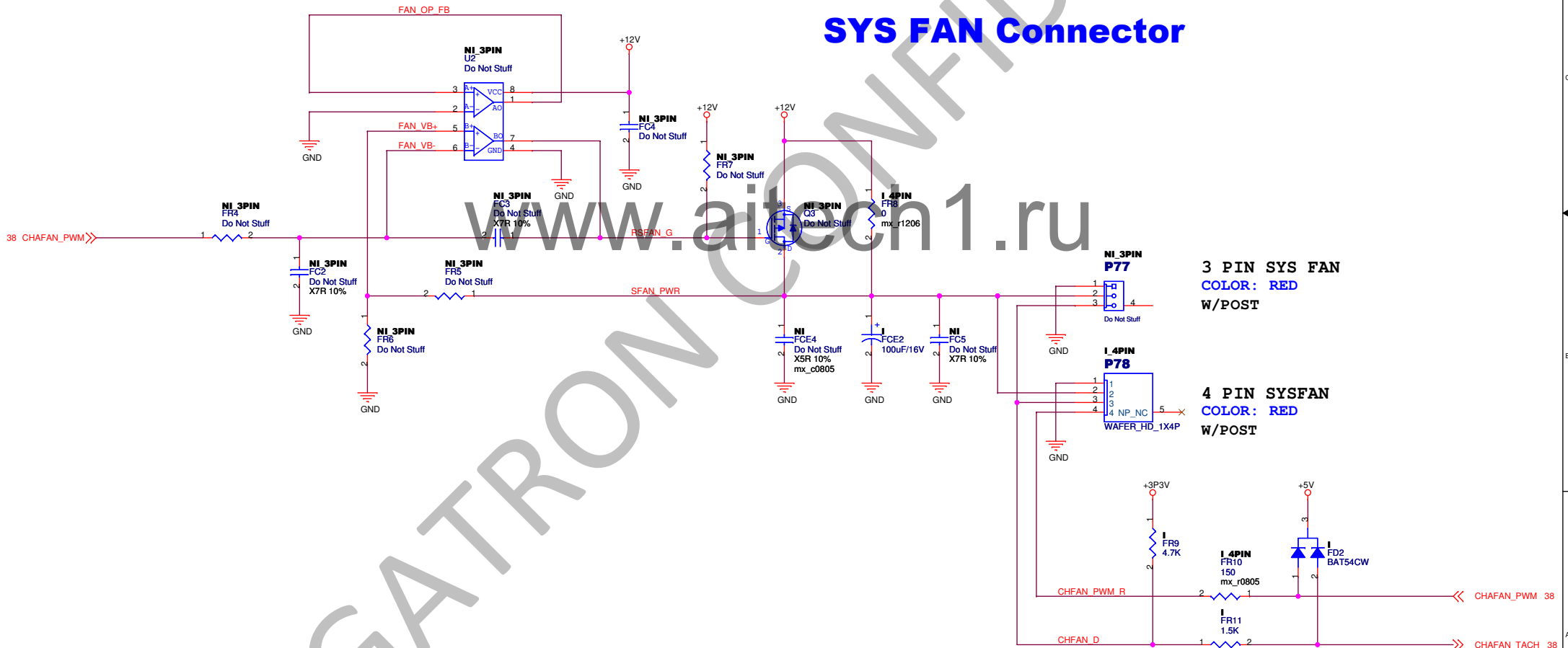
CPU FAN
COLOR: WHITE
W/POST



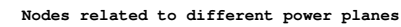
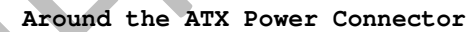
SYS FAN Connector

3 PIN SYS FAN
COLOR: RED
W/POST

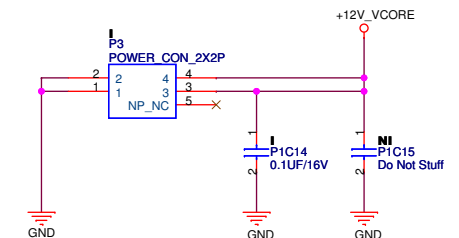
4 PIN SYSFAN
COLOR: RED
W/POST

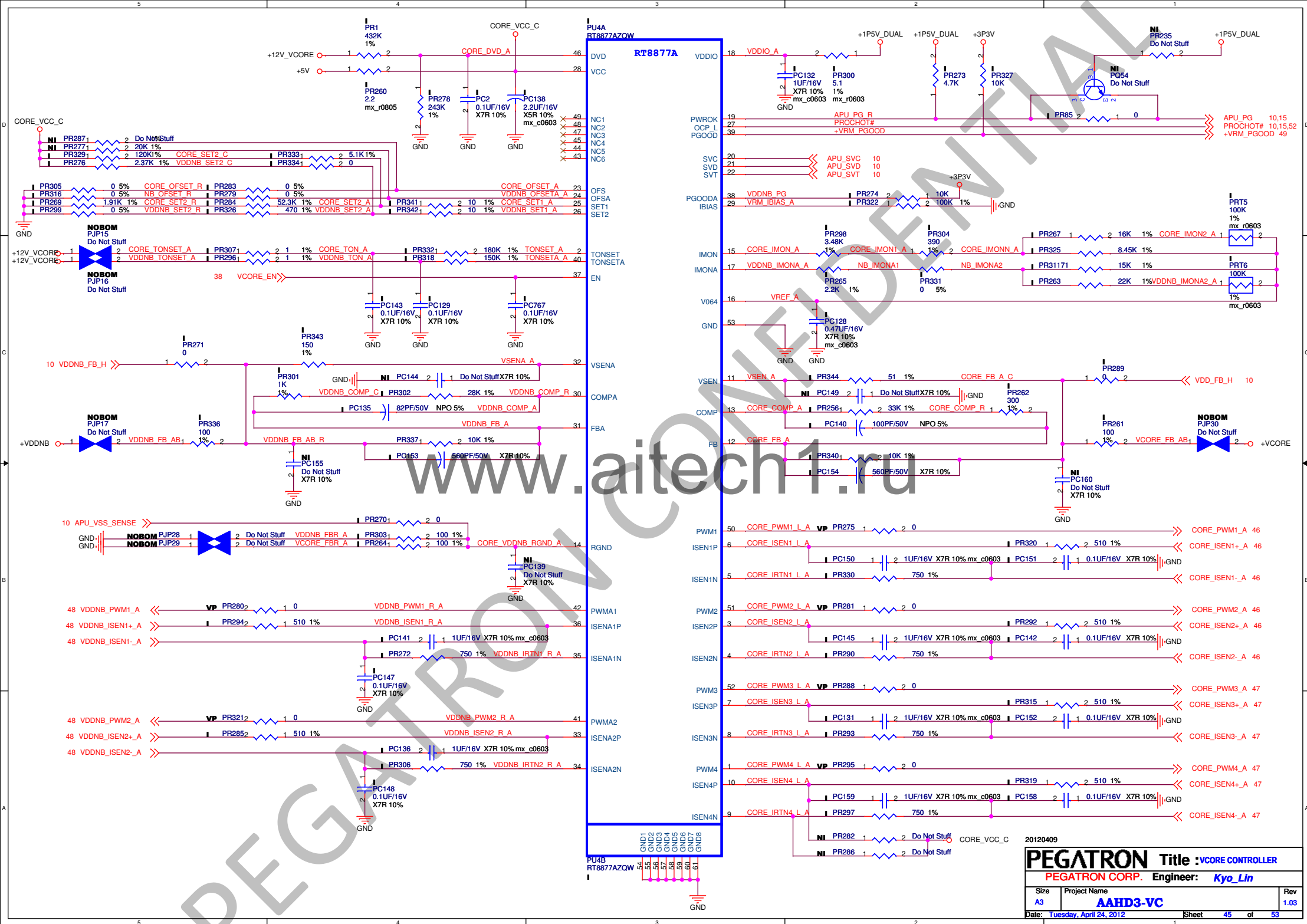


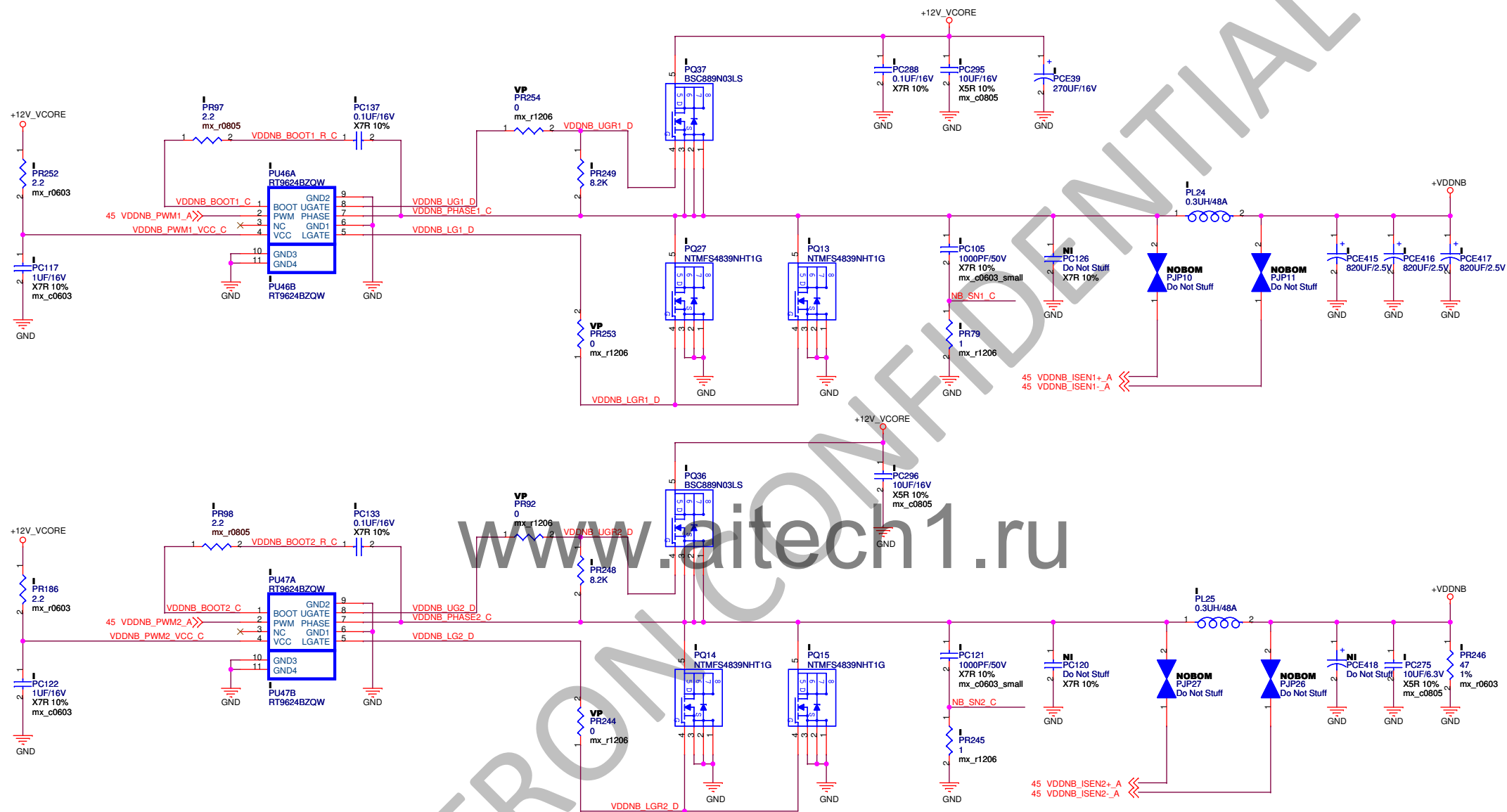
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VRM POWER SUPPLY CONNECTOR

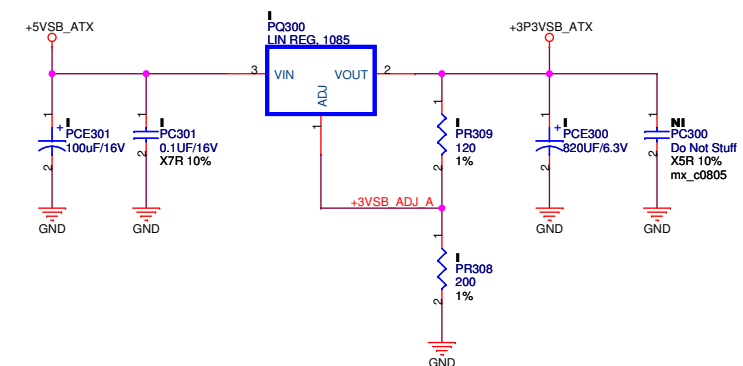


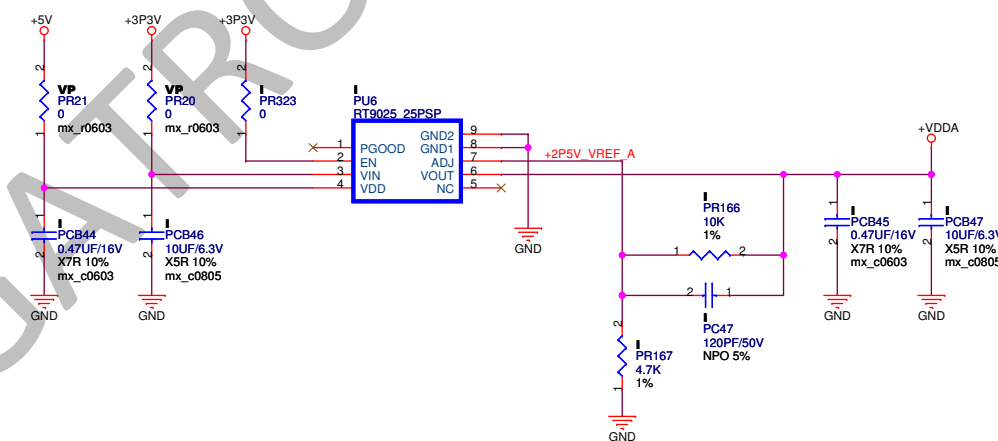
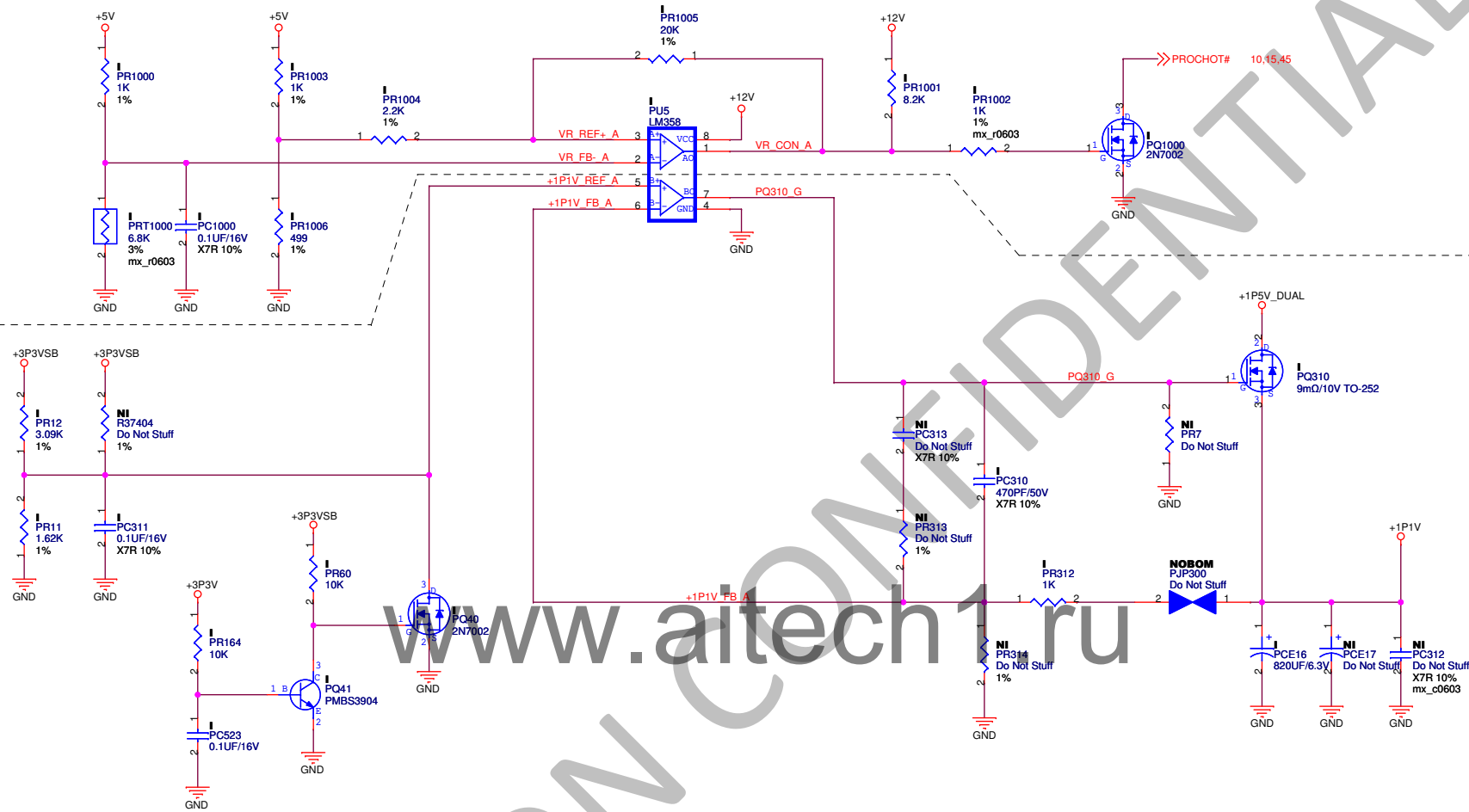




20120409

PEGATRON			Title : VDDNB
PEGATRON CORP.			Engineer: Kyo_Lin
Size	Project Name	Rev	
A3	AAHD3-VC	1.03	
Date: Tuesday, April 24, 2012		Sheet	48 of 53





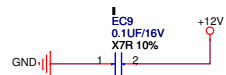
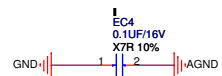
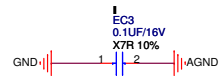
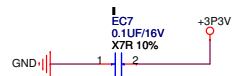
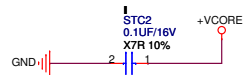
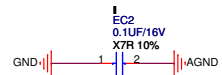
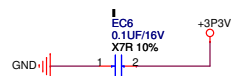
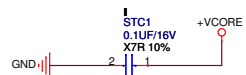
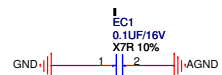
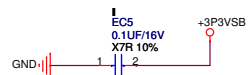
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PEGATRON Title :PROCHOT#& 1P1V& +2P5V

PEGATRON CORP. Engineer: Kyo_Lin

Size A3	Project Name AAHD3-VC	Rev 1.03
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PEGATRON		Title : EMI CAP	
PEGATRON CORP.		Engineer: Kyo_Lin	
Size	Project Name	Rev	
Custom	AAHD3-VC	1.03	
Date: Tuesday, April 24, 2012		Sheet	53 of 53